

CONTROL PREDICTIVO DE CORRIENTE
APLICADO AL FILTRO ACTIVO DE POTENCIA
BASADO EN CONVERTIDORES PUENTE-H
MULTINIVEL



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**CONTROL PREDICTIVO DE CORRIENTE APLICADO AL FILTRO
ACTIVO DE POTENCIA BASADO EN CONVERTIDORES PUENTE-H
MULTINIVEL**

Alfredo Renault
Autor

Prof. Dr. Raúl Gregor
Prof. Dr. Jorge Rodas
Tutores Nacionales

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RAÚL IGMAR GREGOR RECALDE, Universidad Nacional de Asunción, Paraguay

Noviembre 2022

Campus Universitario, Luque, Paraguay

RESUMEN

La principal aportación de esta Tesis Doctoral se centra en el análisis teórico junto con la validación experimental de una propuesta de estrategia de control predictivo de corriente modulado aplicado al Filtro Activo de Potencia trifásico en paralelo (SAPF) basados en convertidores puente-H multinivel en cascada (CHB). El presente documento primeramente aborda el estudio de las estrategias de control aplicados a los SAPFs, enfatizando las ventajas y limitaciones que presentan cada una de ellas, así como las estrategias de modulación aplicadas. Posteriormente se aborda el análisis teórico realizado mediante simulaciones del controlador predictivo propuesto para la compensación de los armónicos de corriente existentes en la red eléctrica, utilizando la estrategia de control predictivo basado en modelo (MPC), para la compensación de armónicos de la corriente de la red eléctrica. Finalmente se presentan los resultados obtenidos de la validación experimental utilizando para ello el controlador dSPACE MicroLabBox. Tanto en las simulaciones como en los resultados experimentales se han obtenido resultados satisfactorios tanto en la medición de la distorsión armónica total de la corriente que circula en la red eléctrica como en la compensación de los armónicos de la corriente.

ALFREDO RENAULT

SUMMARY

The main contribution of this Doctoral Thesis focuses on the theoretical analysis together with the experimental validation of a proposal for a predictive modulated current control strategy applied to the three-phase Shunt Active Power Filter (SAPF) based on multilevel cascade H-bridge converters (CHB). This document first deals with the study of the control strategies applied to SAPFs, emphasizing the advantages and limitations that each one of them presents, as well as the applied modulation strategies. Subsequently, the theoretical analysis carried out through simulations of the predictive controller proposed for the compensation of current harmonics in the electrical network is addressed, using the model-based predictive control strategy (MPC), for the compensation of harmonics current in the power grid. Finally, the results obtained from the experimental validation using the dSPACE MicroLabBox controller are presented. Both in the simulations and in the experimental results, satisfactory results have been obtained both in the measurement of the total harmonic distortion of the current that circulates in the power grid and the compensation of the harmonics current.

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ACRÓNIMOS

AC	Corriente Alterna
APF	Filtro Activo de Potencia
BJT	Transistor de Unión Bipolar
<i>dc</i>	Corriente Continua
DCMC	Convertidor Multinivel con Fijación de Diodos
<i>dc-link</i>	Bus de Continua
DSP	Procesador de Señal Digital
FP	Factor de Potencia
FPGA	Arreglos de Compuertas Lógicas Programables
GTO	Tiristor Desactivado por Compuerta
HVICD	Accionamiento de Circuito Integrado de Alta Tensión
IGBT	Transistor Bipolar de Puerta Aislada
LSPWM	PWM con Desplazamiento de Nivel

MOSFET	Transistor de Efecto de Campo de Semiconductor de Oxido Metálico
MPC	Control Predictivo Basado en Modelo
MSE	Error Cuadrático Medio
MVSI	Inversor de Fuente de Tensión Multinivel
PCC	Punto de Acoplamiento Común
PID	Proporcional, Integral, Derivado
PSPWM	PWM con Desplazamiento de Fase
PWM	Modulación por Ancho de Pulso
SAPF	Filtro Activo de Potencia en Paralelo
SiC	Carburo de Silicio
SIT	Transistor de Inducción Estática
SRF	Marco de Referencia Síncrono
SV	Espacio Vectorial
THD	Distorsión Armónica Total
UPQC	Acondicionador de Calidad de la Energía Unificado
UPS	Sistema de Alimentación Ininterrumpida

CAPÍTULO 1

JUSTIFICACIÓN Y METODOLOGÍA

1.1. Introducción

El estudio de los convertidores electrónicos de potencia ha experimentado un constante crecimiento durante la última década, motivado principalmente por la gran cantidad de aplicaciones industriales que incluyen éstos dispositivos, entre las que sobresalen la movilidad eléctrica, la integración de fuentes de generación de energía eléctrica basadas en fuentes renovables y la mejora de la calidad de la energía eléctrica. En el ámbito de la energía, uno de los tópicos que ha captado un gran interés en la comunidad científica constituye el estudio y aplicación de novedosas estrategias de control aplicados a éstos convertidores, con el objeto de convertir eficientemente la energía y así cumplir con los estándares de conexión a red y calidad de la energía eléctrica. En ese contexto, se han propuesto en la literatura diversas estrategias de control, empezando por las más convencionales, entre las que se encuentran el control por histéresis y el control proporcional-integral-derivativo (PID). Hoy en día, gracias a la evolución y el aumento tanto de la capacidad de microprocesadores como de las tecnologías de procesamiento digital de señales, han permitido la

implementación de avanzados métodos de control diseñados para satisfacer la creciente demanda de los convertidores electrónicos de potencia. Entre ellas, la técnica denominada control predictivo basado en el modelo (MPC) ha demostrado ser una interesante alternativa a los controladores convencionales, principalmente para el control de convertidores electrónicos de potencia y accionamientos electromecánicos. La principal característica del MPC es la utilización del modelo matemático del proceso a controlar de manera a realizar las predicciones futuras de las variables de estado. Entre las ventajas del MPC se pueden mencionar su rápida respuesta, fácil implementación e inclusión de consignas de control. Sin embargo, posee ciertas desventajas como su frecuencia de conmutación variable que ocasiona un esfuerzo desigual a los conmutadores del convertidor y a su vez dificulta el diseño del filtro de salida.

En ese sentido, en esta Tesis Doctoral se propone una estrategia de control predictivo de corriente utilizando la estrategia de modulación por desplazamiento de fase en combinación con el espacio vectorial (SV-PSPWM), aplicado al filtro activo de potencia trifásico en paralelo (SAPFs) basados en convertidores multinivel en configuración puente-H en cascada (CHBs) de 7 niveles, utilizando como generación de referencia el marco referencia síncrono (SRF), para la compensación de armónicos en la red de distribución eléctrica. La propuesta de control fue validada, por un lado, mediante estudios teóricos basados en simulaciones y, por otro, mediante resultados experimentales obtenidos en una bancada especialmente diseñada para el mismo.

1.2. Motivación

Recientemente se han producido un incremento considerable de las cargas no lineales conectadas a los sistemas de distribución de energía, produciendo un deterioro en la calidad de la energía. Asimismo, el aumento de cargas no lineales ocasiona un consumo de corrientes no sinusoidales con un alto contenido en armónicos no deseados. A su vez, éstos armónicos se inyectan a la red eléctrica ocasionando un detrimento de la calidad de la energía eléctrica generada ocasionando un aumento de las pérdidas, desequilibrio de cargas, circulación de corriente por el punto neutro, errores en las medidas de la red, entre otros. No obstante, gracias al gran avance producido en el campo de la electrónica de potencia y del control automático ha permitido hacer frente a los mencionados problemas mediante la utilización de SAPFs, los cuales son capaces de compensar los armónicos no deseados de corriente. Los SAPFs presentan varias ventajas si se los compara con los filtros pasivos, entre los que se mencionan las siguientes: (i) elevada capacidad de adaptación a cambios en la carga o la red (mediante su control automático), (ii) menor sensibilidad a problemas de resonancia al conectarlos a la red, (iii) posibilidad de utilización para otros

objetivos tales como la compensación de la potencia reactiva y el equilibrio de fases. En ese contexto, la presente investigación se enfoca en el estudio de una propuesta de MPC en conjunto con una etapa de modulación aplicado al SAPF para la mejora de la calidad de la energía eléctrica generada. Los objetivos de la presente Tesis Doctoral se presentan a continuación.

1.3. Objetivo general

Aportar al estado del arte del control predictivo aplicado al filtro activo de potencia trifásico utilizando como etapa de conversión un convertidor electrónico de potencia basado en celdas puente-H en cascada.

1.4. Objetivos específicos

- Realizar un análisis teórico del control predictivo de corriente aplicado al SAPF utilizando herramientas de simulación computacional.
- Evaluar el uso combinado de estrategias de modulación con el control predictivo de corriente a fin de mejorar las prestaciones dinámicas en términos de reducción del error cuadrático medio en las variables controladas y mejora en la distorsión armónica en corriente.
- Analizar el uso de estrategias de control predictivo de corriente basadas en soluciones sub-óptimas, enfocadas en la reducción de vectores aplicables en el proceso de optimización del control predictivo, a fin introducir mejoras en términos de reducción del costo computacional y aumento de la frecuencia de muestreo.
- Validar las aportaciones resultantes de la implementación del control predictivo de corriente en aplicaciones de SAPF mediante ensayos experimentales.

1.5. Organización de la Tesis Doctoral

La presente Tesis Doctoral se ha organizado en cinco capítulos con el fin de facilitar la lectura. En ese sentido, se incluye un breve resumen de cada uno de ellos:

Capítulo 1: Justificación y metodología. En este capítulo se introduce la Tesis Doctoral mencionando la motivación que llevó a la realización de la misma, así como el objetivo general y los objetivos específicos.

Capítulo 2: Filtros activos de potencia, modelado y control predictivo. En este capítulo se detalla las principales taxonomías, configuraciones y las estrategias de control aplicadas al APF.

Capítulo 3: Análisis teórico. En este capítulo se detalla el análisis teórico mediante de simulación de la estrategia de control propuesta.

Capítulo 4: Validación experimental del control predictivo aplicado al SAPE. En el presente capítulo se muestra los resultados experimentales de la estrategia de control propuesta.

Capítulo 5: Conclusiones y trabajos futuros. En este capítulo se presenta las conclusiones de la Tesis Doctoral y las líneas futuras de investigación.

CAPÍTULO 2

FILTROS ACTIVOS DE POTENCIA, MODELADO Y CONTROL PREDICTIVO

2.1. Introducción

Los filtros activos de potencia (APFs) constituyen en la actualidad una tecnología madura en lo que respecta a su uso para la compensación de los armónicos de corriente, de la potencia reactiva y de la corriente circulante en el punto neutro en redes de distribución eléctrica de corriente alterna. Adicionalmente, los APFs han evolucionado mediante desarrollo de configuraciones variables, nuevas estrategias de control y el uso de dispositivos de estado sólido tales como los SiC-MOSFETs [1], [2]. Entre otras aplicaciones de los APFs se encuentra la mitigación del parpadeo de voltaje en sistemas trifásicos [3], [4]. Estos objetivos se logran individualmente o en combinación según los requisitos, tanto la estrategia de control como la topología del convertidor que deben seleccionarse adecuadamente [5], [6].

El uso generalizado de los convertidores electrónicos de potencia en el proceso de conversión de la energía eléctrica ha motivado que los problemas relacionados con la calidad de la energía hayan cobrado mayor relevancia [7], [8]. En ese sentido, es posible

encontrar publicaciones científicas que se enfocan en el mejoramiento de la calidad de la energía eléctrica así como la búsqueda de la causa y del efecto de los armónicos presentes en las redes eléctricas, entre otros [9], [10]. El APF se considera un dispositivo ideal para mitigar los problemas de calidad de la energía ocasionadas principalmente por las cargas no lineales. Es importante mencionar que algunas cargas monofásicas, tales como las luces domésticas, hornos, televisores, suministros de energía para computadoras, acondicionadores de aire y impresoras láser, se comportan como cargas no lineales y causan problemas de calidad de energía [11], [12].

Se han investigado diferentes configuraciones y estrategias de control de los APFs monofásicos de dos hilos con el objeto de satisfacer las necesidades de cargas monofásicas no lineales. Además, desde comienzos de los años 70, se han desarrollado y comercializado muchas configuraciones de APFs en sistemas de alimentación ininterrumpida (UPS). Tanto el convertidor de fuente de corriente (con almacenamiento de energía inductiva) como el convertidor de fuente de voltaje (con almacenamiento de energía capacitiva) se utilizan para en aplicaciones de APF monofásicos [13], [14]. A partir de 1976, en el desarrollo de APF trifásicos se han abordado diversas estrategias de control entre las que resaltan la teoría de la potencia reactiva instantánea (IRPT), la teoría $d - q$ del marco de referencia síncrono (SRF), el método de detección síncrona y el método de filtro de muesca [15], [16].

Por otro lado, el problema de la excesiva corriente neutra se observa en sistemas trifásicos de cuatro hilos principalmente debido a las cargas desequilibradas no lineales producidas por fuentes de alimentación de computadoras, luces fluorescentes, entre otros. Estos problemas de corriente neutra y corrientes de carga desequilibradas en sistemas de cuatro hilos se han intentado resolver mediante la eliminación o la reducción de la corriente neutra, la compensación de armónicos, el equilibrio de carga y la compensación de potencia reactiva [17], [18].

Uno de los principales hitos que produjo un importante avance de la tecnología APF fue la llegada de dispositivos de estado sólido [19]. En las etapas iniciales, se han utilizado tiristores, transistores de unión bipolar (BJT) y transistores de efecto de campo de semiconductores de óxido de metal (MOSFET) de potencia para implementar los APFs. Posteriormente se han empleado transistores de inducción estática (SIT) y los tiristores desactivados por compuerta (GTO). Con la introducción de los transistores bipolares de puerta aislada (IGBT), la tecnología APF ha recibido un gran impulso y en la actualidad se considera uno de los mejores dispositivos de estado sólido para su uso en APF [20], [21]. La tecnología a los dispositivos de medición (sensores) también ha contribuido a la mejora del rendimiento del APF [22], [23].

El siguiente avance en el desarrollo de los APFs ha sido fruto del resultado de la revolución de la microelectrónica. A partir del uso de componentes electrónicos la evolución

ha sido beneficiado a los microprocesadores, microcontroladores y los dispositivos de procesamiento digitales (DSPs) [24], [25]. En la actualidad es posible implementar complejos algoritmos en tiempo real para el control del APF a un costo económico razonable. Este desarrollo en el campo del APF ha hecho posible el uso de diferentes algoritmos de control, como control proporcional-integral (PI), control de estructura variable, control de lógica difusa y algoritmos de control basados en redes neuronales para mejorar el rendimiento dinámico en régimen permanente del APF. Con estas mejoras, los APFs son capaces de proporcionar una acción correctiva rápida incluso con cargas no lineales que cambian dinámicamente [26], [27].

2.2. Taxonomía de los APFs

Según los problemas de calidad de energía que se desea solucionar se selecciona el tipo de APF adecuado. En ese sentido, los APFs se clasifican en cuatro, el APF paralelo, que es utilizado para mejora de la corriente eléctrica en la red de distribución, APF en serie, para mejora de la calidad de voltaje en la red de distribución, APF híbrido, que es la combinación del APF paralelo y serie, y los acondicionadores de calidad de energía unificado (UPQC) [28], [29].

El SAPF funciona inyectando corriente armónica en el sistema, de magnitudes como las corrientes armónicas generadas por una carga no lineal dada, pero con fases opuestas para mantener una corriente sinusoidal en el punto de acoplamiento común (PCC) [30]. El principal objetivo del SAPF es compensar corrientes armónicas a fin de dar una mejora al factor de potencia, la distorsión armónica total (THD) de la red de distribución eléctrica, compensación de potencia reactiva, las corrientes desequilibradas y la compensación de la corriente en el punto neutro [31], [32]. En el esquema de la **Figura 2.1** se observan los distintos tipos de APFs y se resalta la topología utilizada en esta tesis. A continuación de detallan el funcionamiento de cada configuración del APF.

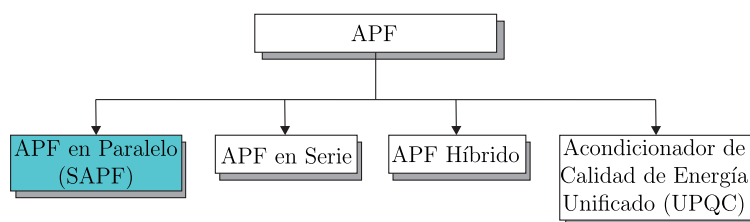


Figura 2.1 Configuraciones de APF para mejorar la calidad de la energía [33].

APF en serie. Los APFs conectados en serie con la fuente generadora de armónicos se comportan como una fuente de voltaje en serie con la propia red. Se conecta antes de la carga y en serie con la alimentación, a través de un transformador, de tal manera a eliminar los armónicos de voltajes y así balancear y regular el voltaje en los terminales de la carga o la línea [34], [35].

Acondicionador de calidad de energía unificado (UPQC). Esta configuración combina el APF en paralelo con el APF en serie. El APF en paralelo cancela los armónicos de corriente y puede compensar la energía reactiva, mientras que el APF en serie realiza la función de desacoplamiento a la red y además puede realizar otras funciones tales como la regulación de voltaje, compensación de las variaciones de voltaje (flickers) y equilibrado de fases en el punto de conexión a la red [36].

APF híbrido. El APF híbrido consta de un sistema de filtrado pasivo convencional apoyado por un APF situado en diferentes posiciones en relación con el filtro pasivo. Esta combinación optimiza el sistema de cancelación pasiva, además de evitar los problemas de resonancias entre los componentes del filtro pasivo y la impedancia de línea y permite potencias de filtrado elevadas a un costo inferior al del filtrado activo puro [37], [38]. Por otro lado, dependiendo de la interconexión realizada entre el sistema de filtro pasivo y el sistema de APF, pueden considerarse las siguientes estructuras básicas: APF en serie con la línea, APF en serie con el filtro pasivo, APF en paralelo con la línea y la carga, y finalmente APF en serie con la línea y el filtro pasivo [39], [40].

APF paralelo (SAPF). Los SAPF se utilizan para la compensación de las corrientes armónicas y la corrección del factor de potencia se muestra en la **Figura 2.2**. Idealmente, para reducir las componentes oscilatorias de la potencia que circulan entre la fuente y las cargas, tanto el voltaje como la corriente deben ser del tipo sinusoidales, en fase y equilibrados [41]. Por lo tanto, la red eléctrica puede funcionar de manera eficiente y con una mejor calidad de energía, evitando problemas referentes a la potencia reactiva, los armónicos y el desequilibrio en la red eléctrica [42]. Sin embargo, en casos generales, debido a las cargas que normalmente son del tipo inductivas y no lineales, así como al desequilibrio de las cargas conectadas a las diferentes fases de una red trifásica, existirá una potencia reactiva y, consecuentemente, formas de onda de corriente distorsionadas debido al desequilibrio así como la presencia de armónicos [43].

2.3. El convertidor multinivel CHB como interfaz de potencia

En la actualidad existen cada vez más aplicaciones demandan mayor potencia o voltaje, para alcanzar altos niveles de potencia es necesario que los VSIs sean capaces de aumentar

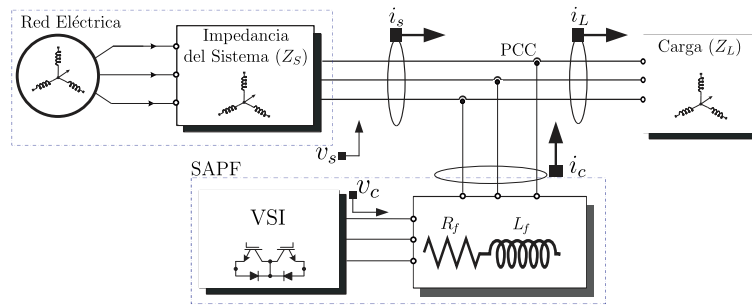


Figura 2.2 Esquema de conexión del SAPF.

su voltaje de operación a niveles que actualmente sobrepasan los impuestos por la tecnología de los semiconductores. Una posible solución es la conexión en serie de VSI en las topologías de dos niveles y así aumentar el voltaje nominal del inversor [44]. Además es habitual que exista una distribución no equitativa del voltaje entre los dispositivos conectados en serie, lo que conduce a una reducción de la potencia de los dispositivos y a una menor confiabilidad debido a posibles sobrevoltajes en un dispositivo [45]. Esta es la razón por la que las topologías de VSIs actuales fueron la única alternativa para aplicaciones de alta potencia durante varias décadas [46].

Los VSIs multinivel se desarrollaron especialmente para obtener voltajes más elevados. En lugar de conectar varios IGBTs (o similares) en serie, las estructuras de inversores multinivel organizan los semiconductores con capacitores adicionales que subdividen el de voltaje total del convertidor hasta el límite de bloqueo del semiconductor [47].

Estas propiedades hacen que los inversores multinivel sean muy atractivos para aplicaciones de alta potencia (1 MW a 50 MW), que alcanzan el nivel de voltaje medio (2,3 kV a 10 kV), como bombas, ventiladores, transportadores, tracción de alta velocidad y propulsión de barcos, por nombrar algunos [48]. Actualmente varias topologías han encontrado aceptación industrial y son comercializadas por varios fabricantes de convertidores de media tensión, a pesar del nivel de madurez que han alcanzado estos inversores, los convertidores multinivel tienen una estructura de circuito más compleja, con más semiconductores, por lo tanto, más estados de conmutación u opciones de control, que en conjunto presentan varios desafíos técnicos [49]. Sin embargo, éstos estados de conmutación adicionales también permiten un gran número de posibilidades y grados de libertad adicionales [50]. Esta es la razón por la cual las nuevas topologías y los métodos de modulación todavía están bajo investigación y desarrollo muy activos [51]. Esta sección presenta una breve descripción de las topologías de convertidores multinivel más comunes y los métodos de modulación multinivel utilizados en la industria [52].

Hay una gran cantidad de topologías de convertidores multinivel reportadas en la literatura, pero las topologías de convertidores multinivel más comunes en la industria son los convertidores con abrazadera de diodo, también llamados convertidores con punto neutro de fijación (NPC), CHB y el inversor de capacitor flotante (FCI) [53]. En la **Figura 2.3** se representa una clasificación de las topologías de convertidores multinivel, que incluye estos tres convertidores junto con topologías introducidas más recientemente, algunas de ellas derivadas de los inversores multinivel convencionales [54].

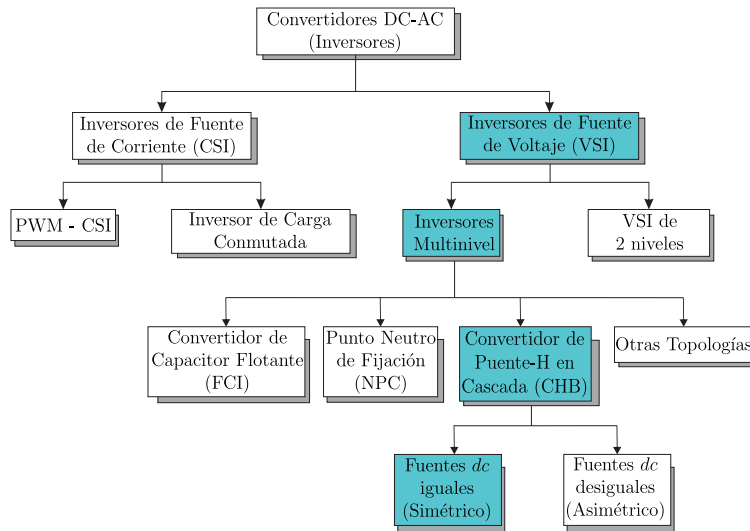


Figura 2.3 Tipos de convertidores aplicados a APFs [55].

2.3.1. Inversores NPC

El inversor multinivel NPC se introdujo a principios de 1980, este convertidor se basó en una modificación de la topología clásica del VSI trifásico de dos niveles [56]. En el VSI convencional de dos niveles, cada semiconductor de potencia debe soportar un esfuerzo de voltaje igual a V_{dc} . La modificación para obtener el convertidor NPC de tres niveles agrega dos semiconductores adicionales por fase y dos diodos de fijación que dividen el dc -link por la mitad. Usando esta nueva topología, cada dispositivo de conmutación bloquea como máximo un voltaje igual a $V_{dc}/2$. Entonces, si estos semiconductores tienen las mismas características que los utilizados en el VSI de dos niveles, el voltaje de dc -link puede duplicarse teóricamente, lo que lleva a duplicar la potencia nominal del convertidor [57].

La topología NPC se puede extender para lograr más niveles en los voltajes de fase de salida, para lo cual se conectan más capacitores en serie en el *dc-link*, y se usan interruptores y diodos de fijación adicionales para fijar los interruptores a cada capacitor [58]. Por lo tanto, en este caso se denomina más correctamente un convertidor con abrazadera de diodo, ya que no solo hay un nodo de abrazadera en el lado del *dc-link*, e incluso no necesariamente un punto neutral con potencial de cero voltios (este es el caso incluso para niveles) [59]. Sin embargo, la topología NPC con un alto número de niveles tiene una distribución muy desigual de las pérdidas entre los semiconductores, lo que obliga a reducir la potencia de los dispositivos y también a reducir la vida útil de los semiconductores de potencia [60].

2.3.2. Inversores FCI

La topología del convertidor FCI multinivel se desarrolló en la década de 1990 y utiliza varios capacitores flotantes en lugar de diodos de fijación para compartir el voltaje entre los dispositivos y lograr diferentes niveles de voltaje en la salida [61]. Se pueden utilizar otras relaciones de voltaje para los capacitores flotantes, aumentando el número de niveles, sin embargo, esto hace que el equilibrio de voltaje de los capacitores sea más difícil e impone diferentes voltajes de bloqueo entre los dispositivos y, por lo tanto, no encuentra aceptación industrial [62].

2.3.3. Inversores multinivel CHB

El convertidor CHB es una estructura muy utilizada en aplicaciones de potencia, no posee un *dc-link* único como tal, sino mas bien posee varias fuentes de *dc*. Los convertidores multinivel fueron desarrollados desde mediados de 1980, inicialmente con el trabajo de Nabae, Takahashi y Akagi en el año 1988 [63]. Esta topología se implementa mediante la interconexión de etapas puente-H independientes, en la **Figura 2.4** se observa un esquema de convertidor CHB de 7 niveles, realizada mediante la interconexión en serie de 3 módulos de CHB independientes [64], [65].

El convertidor multinivel en su topología CHB presenta varias ventajas con respecto a la de dos niveles, el CHB permite un diseño escalable debido a la estructura idéntica de cada CHB, que además implica un proceso de fabricación más rápido y de bajo costo [66], [67]. Requiere un menor número de componentes considerando que no hay diodos extra de sujeción o capacitor de equilibrado de voltaje para lograr el mismo número de niveles de voltaje [68]. El potencial de descarga eléctrica se reduce debido a las fuentes *dc* separadas [69].

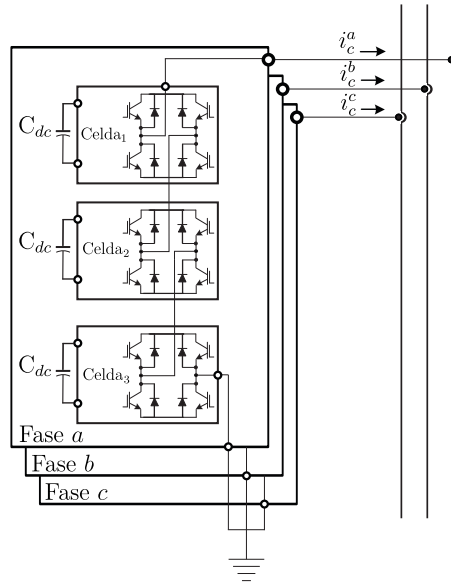


Figura 2.4 Esquema del CHB multinivel.

Por otro lado se puede mencionar algunas desventajas, tales como la necesidad de fuentes de dc separadas para cada uno de los CHB [70]. La modulación de conmutación necesita ser optimizada para aplicaciones de alto rendimiento, debido a una combinación limitada de patrones de conmutación [71]. Para el intercambio de potencia reactiva, el pulso de potencia debe ser el doble de la frecuencia de salida, en consecuencia el dc -link de cada CHB requiere un sobredimensionamiento de los capacitores del dc -link [72], cada CHB posee corrientes desiguales, requiere un mayor costo computacional, por mencionar algunos [73].

Para el funcionamiento correcto de esta topología es necesario que los voltajes de los dc -link sean independientes y estén aisladas entre sí, lo cual se implementa mediante capacitores. Para incrementar el número de niveles es necesario conectar más celdas en cascada, siendo el voltaje de salida del convertidor la suma o combinación de cada uno de los voltajes que las diferentes celdas aporten [74, 75]. Las topologías de puente-H multinivel se pueden dividir en dos categorías según la dependencia de la relación de los voltajes que maneje cada puente-H: simétricas o asimétricas. Se consideran simétricas si los voltajes de dc -link de todos los puentes son iguales entre sí o asimétricas a aquellas cuyos voltajes de dc -link son diferentes. Lo más habitual es encontrar voltajes con relaciones 1:2 o 1:3 [64].

La mayor ventaja de la que goza esta topología es su modularidad, gracias a ella se puedan construir convertidores con un número de niveles muy elevado. En contrapartida, su mayor inconveniente es la necesidad de que los voltajes de alimentación de cada celda sean independientes [76]. Será necesario, por lo tanto, el empleo de tantas fuentes aisladas como celdas tenga el convertidor, para aplicaciones en las que no se manipule potencia activa (filtrado activo, compensación de reactiva, etc.). Si se eligen adecuadamente los estados redundantes de conmutación de los interruptores, se puede controlar la carga de los capacitores y, por lo tanto, evitar el uso de fuentes aisladas [77]. En esta Tesis se ha optado con la configuración CHB multinivel de 7 niveles.

2.4. Modelo matemático del SAPF

La **Figura 2.5 (a)** muestra la propuesta SAPF basada en un convertidor CHB trifásico de 7 niveles, que consiste en tres celdas de puente-H en cascada por fase. Las diferentes celdas del puente-H tienen un enlace de dc independiente (C_{dc}). Cada celda contiene cuatro dispositivos de conmutación, lo que da como resultado un total de 36 interruptores de alimentación. En consecuencia, se necesitan cuatro señales de conmutación (Sf_{ij}^ϕ) para controlar cada celda, donde ϕ representa la fase (a, b y c), i el número de celda en la fase correspondiente (1, 2 o 3) y j el dispositivo de conmutación correspondiente a la celda (1, 2, 3 o 4), respectivamente [78]. La **Tabla 2.1** muestra las combinaciones permitidas de señales de activación y los respectivos voltajes de salida correspondientes a la Celda₁ de la fase “ a ”, donde C_{dc} es el voltaje del capacitor. Se definen combinaciones similares permitidas para las otras celdas. No se permiten otras combinaciones posibles porque provocan un cortocircuito en el dc -link de la celda. Para evitar esto, solo se utilizan dos señales de activación y sus niveles complementarias como se muestra en la **Figura 2.5 (b)** para el caso particular de la Celda₁.

El modelo dinámico de la configuración del circuito **Figura 2.5 (a)** se puede obtener usando las leyes del circuito de Kirchhoff. Para fines de modelado, se supone que las fuentes de voltaje trifásicas están balanceadas y que todos los módulos tienen la misma

Tabla 2.1 Combinaciones de señales de activación permitidas para una celda CHB.

Sa_{11}	Sa_{13}	Sa_{12}	Sa_{14}	v_c^a
1	0	0	1	$+v_{dc}$
1	1	0	0	0
0	0	1	1	0
0	1	1	0	$-v_{dc}$

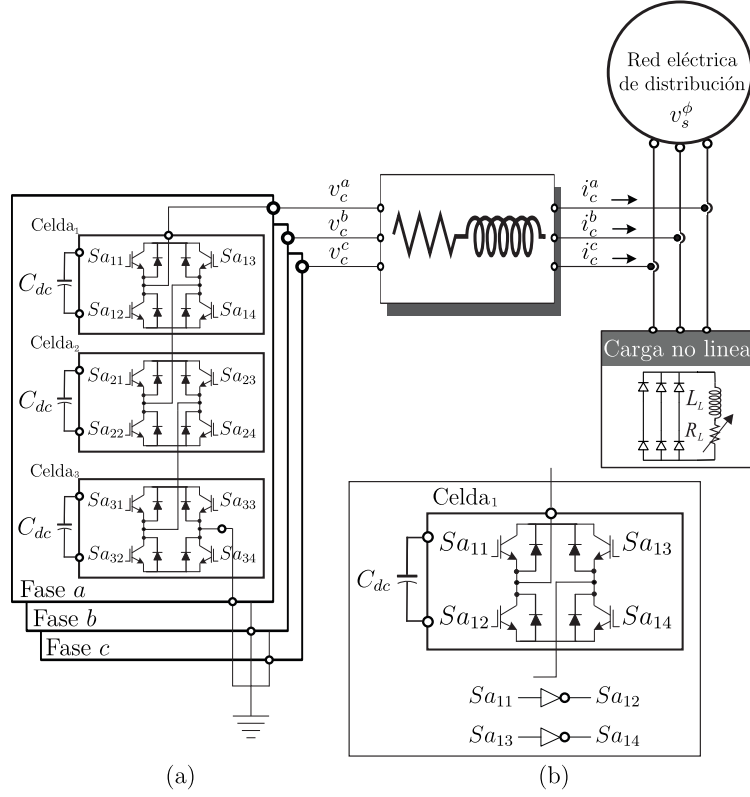


Figura 2.5 Sistema SAPF basado en convertidor CHB trifásico de 7 niveles.

capacitancia y voltaje en su lado de dc . El SAPF basado en convertidor CHB está conectado en el PCC. Aplicando la ley de voltaje de Kirchhoff para el lado ac del SAPF, se obtienen las siguientes ecuaciones:

$$\frac{di_c^\phi}{dt} = \frac{v_s^\phi}{L_f} - \frac{R_f}{L_f} i_c^\phi - \frac{n_c S f_{ij}^\phi v_{dc}^\phi}{L_f} \quad (2.1)$$

$$\frac{dv_{dc}^\phi}{dt} = \frac{S f_{ij}^\phi i_c^\phi}{C_{dc}} - \frac{v_{dc}^\phi}{R_{dc} C_{dc}} \quad (2.2)$$

donde n_c es el número de celdas, R_{dc} es una resistencia conectada en paralelo al capacitor C_{dc} que concentra las pérdidas totales en el lado dc , $S f_{ij}^\phi$ es la función de conmutación y la resistencia R_f es la resistencia parásita (serie) del inductor L_f .

2.5. Clasificación de las estrategias de control aplicadas al SAPF

En las últimas décadas el uso de convertidores de potencia se ha vuelto muy popular teniendo una amplia gama de aplicaciones como accionamientos eléctricos, conversión de energía, tracción y generación distribuida [79]. El control de convertidores de potencia ha sido ampliamente estudiado, obteniéndose nuevos esquemas de control, entre los que se puede clasificar según la **Figura 2.6**. A continuación se describen los mas relevantes.

2.5.1. Controladores clásicos

Control lineal. Esta técnica está bien establecida en la literatura y es ampliamente implementada en aplicaciones prácticas. Esta técnica utiliza un control PI el cual linealiza el modelo matemático del convertidor de potencia que originalmente tiene un modelo matemático no-lineal [80]. El controlador PI procesa el error de corriente y produce un voltaje de referencia para usar con la etapa de modulación [81].

Histéresis. El control de histéresis se reconoce como una técnica de control no lineal, el cual las corrientes medidas se comparan con sus respectivas corrientes de referencias [82]. El relé en cada fase determina las señales de conmutación de manera que las cargas medidas se limitan dentro de los límites de banda superior e inferior establecidos por el ancho de banda de histéresis σ definido por el usuario [83].

Lógica difusa. Es una técnicas de control no lineal y el mejor entre los controladores adaptativos. El error de seguimiento de referencia de la corriente de carga y su derivado se utilizan como entrada para el controlador difuso, que a su vez incorpora la experiencia, el conocimiento y la intuición del diseñador en forma de funciones de pertenencia y reglas de control “if-then”[84]. Dado que los convertidores de potencia son de naturaleza no lineal, la robustez del sistema durante las variaciones de los parámetros se puede mejorar utilizando el controlador difuso incluso sin conocer el modelo exacto del convertidor y sus parámetros. Este esquema de control necesita un modulador para la activación de las señales de conmutación [85].

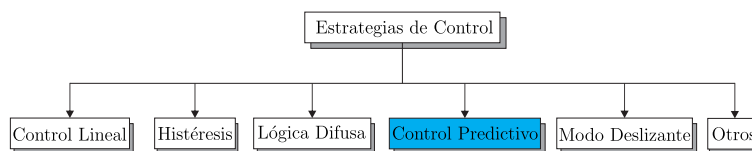


Figura 2.6 Estrategias de control aplicadas al SAPF.

Modo deslizante. El control en modo deslizante (SMC) requiere el modelo del convertidor y los parámetros del sistema. Es una técnica de control digital avanzada y pertenece a la familia de control de estructura variable y control adaptativo [86]. Esta técnica de control puede ser discreta y trata adecuadamente la naturaleza no lineal del convertidor de potencia. Los errores de corriente son procesados por SMC, que en consecuencia genera las referencias de tensión de carga [87]. La variable de control es forzada a seguir o deslizarse a lo largo de la trayectoria predefinida [88]. La estructura del controlador se cambia intencionalmente de acuerdo con una ley de control de estructura preestablecida para lograr una respuesta robusta y estable durante las variaciones de los parámetros del sistema y las perturbaciones de la carga [89].

Control predictivo El control predictivo presenta varias ventajas que lo hacen adecuados para el control de convertidores de potencia. Es intuitivo y fácil de entender, se puede aplicar a una variedad de sistemas, las restricciones y las no linealidades pueden ser fácilmente incluidas [90]. Puede considerarse casos multivariables, y el controlador es fácil de implementar, requiere una gran cantidad de cálculos, en comparación con un esquema de control clásico; sin embargo, los microprocesadores rápidos disponibles hoy en día es posible implementar del control predictivo. En general, la calidad del controlador depende de la calidad del modelo [91].

Otros Entre otros controles se pueden mencionar el control inteligente, que incluye varias técnicas de control, como lógica difusa [92], redes neuronales [93] y algoritmos genéticos [94].

2.6. Estrategias de control predictivo aplicadas al SAPF

El control predictivo constituye una clase muy amplia de controladores que han encontrado una aplicación bastante reciente en convertidores de potencia. La clasificación propuesta en este documento para diferentes controles predictivos se muestra en la **Figura 2.7**.

Entre los objetivos buscados mediante las diferentes estrategias de conmutación se tiene la minimización de los niveles de armónicos de las señales de salida del convertidor, regulación de la amplitud y frecuencia de salida así como el equilibrio de los voltajes en los capacitores del *dc-link*, siempre y cuando la topología y la implementación lo requieran [60], [74].

En este enfoque se toma en cuenta la naturaleza discreta de los conversores para implementar el MPC. El problema de optimización puede ser simplificado y reducido a las predicciones del comportamiento del sistema para los posibles estados de conmutación. Entonces, cada predicción es evaluada en una función de costo y el estado que la minimice

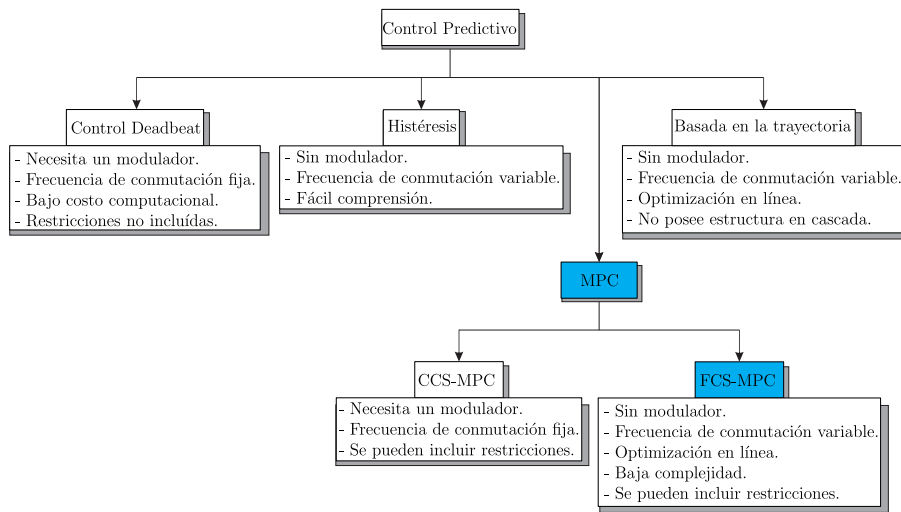


Figura 2.7 Estrategias de control predictivo aplicadas al SAPF [81].

es seleccionado [95], [96]. Como se tiene un número de acciones de control finita, este enfoque se denomina MPC de estado finito (FCS-MPC) [39], [41]. Este esquema de control no requiere el uso de un modulador, lo cual reduce de gran manera la complejidad de implementación. Esta técnica de control ha sido aplicada en un amplio rango de convertidores como los VSI de dos niveles trifásicos [97], NPC [98], FCI [99], back to back [100], CHB [101], convertidores matriciales [102], entre otros [103].

Una de las características del MPC es la posibilidad de incluir múltiples objetivos en el diseño del controlador [104], [105]. En convertidores esto se puede aplicar al control de corriente, control de voltaje, control de torque y flujo, control de potencia, reducción de frecuencia de conmutación, etc. Para cumplir con la consigna de control deseada, sólo es necesario modificar la función de coste [106].

2.7. El control predictivo de corriente aplicado al SAPF

En esta sección se detallan los distintos tipos de control predictivo aplicado a los SAPFs, así como los principales esquemas de generación de referencia.

2.7.1. Modelo de predicción del SAPF

El modelo predictivo se puede obtener a partir de (2.1) utilizando el método de discretización de Euler en adelante. El método de Euler es el método explícito más básico

para la integración numérica de ecuaciones diferenciales ordinarias y, en consecuencia, conlleva una carga computacional baja, lo que beneficia la implementación experimental. El modelo de tiempo discreto SAPF está dado por:

$$i_c^\phi(k+1) = \left(1 - \frac{R_f T_s}{L_f}\right) i_c^\phi(k) + \frac{T_s}{L_f} (v_c^\phi(k) - v_s^\phi(k)) \quad (2.3)$$

donde k representa el instante de muestreo de tiempo discreto real, T_s es el tiempo de muestreo e $i_c^\phi(k+1)$ es la predicción de corrientes de fase SAPF realizadas en la muestra $k+1$. Además, en (2.3), $i_c^\phi(k)$ corresponde a la corriente medida en el filtro de salida en el tiempo de muestreo actual k . Mientras que $v_s^\phi(k)$ corresponde al voltaje de fase medida en la red eléctrica y $v_{dc}^\phi(k)$ representa el voltaje de salida del SAPF en el mismo tiempo de muestreo k . Luego, estos valores medidos son utilizados por el controlador predictivo.

Los esquemas de control aplicado al SAPF se centran en la generación de la corriente de referencia de tal manera a compensar los armónicos de corriente de la red eléctrica. Existen varias técnicas utilizadas para la generación de la corriente de referencia tanto en el dominio de la frecuencia como en el dominio del tiempo, a continuación se presenta las estrategias mayormente utilizadas en el SAPF.

2.7.2. Generación de referencia aplicado al SAPF basado en la teoría IRPT

El esquema de control basada en la teoría IRPT fue propuesto por primera vez por H. Akagi en 1983 [107], utiliza los voltajes trifásicos medidos y las corrientes de carga, para luego transformar a magnitudes bifásicas en el marco de referencia $\alpha - \beta$ utilizando la transformación de Clarke, propuesta por Edith Clarke en 1951 [108]. En la **Figura 2.8** se muestra el esquema de control IRPT aplicado al SAPF. Los voltajes trifásicos y las corrientes de carga se miden y son utilizadas para calcular la potencia reactiva y activa con sus componentes armónicos, para luego aplicar un filtro paso bajo (LPF) antes de su transformación. De esta manera se filtra la componente ac , para luego aplicar la transformación inversa y obtener las corrientes de referencia.

Los voltajes de la red trifásicos son transformados a los marcos de referencia ortogonales $\alpha - \beta$ bifásicas, denotados como $v_{s\alpha}$ y $v_{s\beta}$:

$$\begin{bmatrix} v_{s\alpha} \\ v_{s\beta} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & \frac{1}{2} \\ 0 & \sqrt{\frac{3}{2}} & -\sqrt{\frac{3}{2}} \end{bmatrix} \begin{bmatrix} v_s^a \\ v_s^b \\ v_s^c \end{bmatrix} \quad (2.4)$$

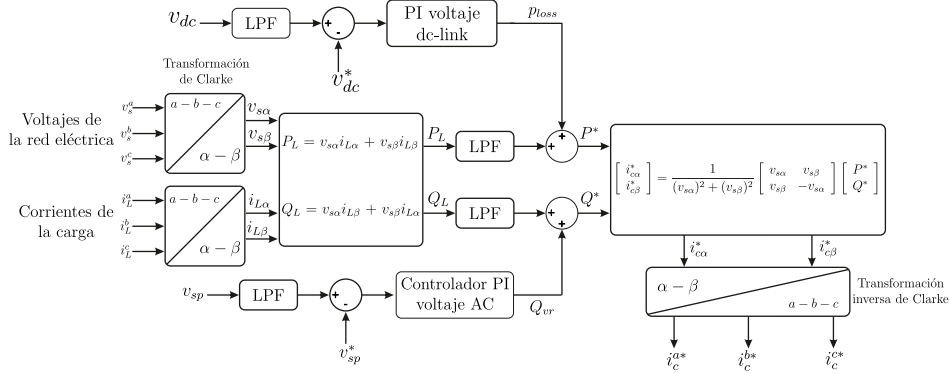


Figura 2.8 Generación de referencia del SAPF utilizando el esquema IRPT.

Análogamente, las corrientes de carga trifásica (i_{La} , i_{Lb} , i_{Lc}) se transforman a los marcos de referencia ortogonales $\alpha - \beta$, denominadas $i_{L\alpha}$ e $i_{L\beta}$ como:

$$\begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & \frac{1}{2} \\ 0 & \sqrt{\frac{3}{2}} & -\sqrt{\frac{3}{2}} \end{bmatrix} \begin{bmatrix} i_L^a \\ i_L^b \\ i_L^c \end{bmatrix} \quad (2.5)$$

Luego, a partir de las expresiones de voltajes y corrientes en el marco de referencia $\alpha - \beta$, la potencia activa instantánea P_L y la potencia reactiva instantánea Q_L de la carga se calculan como:

$$\begin{bmatrix} P_L \\ Q_L \end{bmatrix} = \begin{bmatrix} v_{s\alpha} & v_{s\beta} \\ v_{s\beta} & -v_{s\alpha} \end{bmatrix} \begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \end{bmatrix} \quad (2.6)$$

la potencia instantánea activa P_L puede subdividirse en las potencias $\bar{p}_L$ y $\tilde{p}_L$, que representan al valor medio de la potencia activa y a la componente armónica de dicha potencia, respectivamente. Análogamente, $\bar{q}_L$ y $\tilde{q}_L$ representan al valor medio de la potencia reactiva y la componente armónico de la potencia reactiva, respectivamente. Por lo tanto, estos pueden expresarse como:

$$\begin{aligned} P_L &= \bar{p}_L + \tilde{p}_L \\ Q_L &= \bar{q}_L + \tilde{q}_L \end{aligned} \quad (2.7)$$

Las componentes ac ($\tilde{p}_L$ y $\tilde{q}_L$), de las potencias activa y reactiva se extraen utilizando LPFs y las corrientes de referencia trifásicas (i_s^{a*} , i_s^{b*} e i_s^{c*}), se obtienen mediante la

siguiente ecuación:

$$\begin{bmatrix} i_c^{a*} \\ i_c^{b*} \\ i_c^{c*} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_{s\alpha} & v_{s\beta} \\ -v_{s\beta} & v_{s\alpha} \end{bmatrix}^{-1} \begin{bmatrix} P^* \\ Q^* \end{bmatrix} \quad (2.8)$$

En la **Figura 2.8** se observa que las potencias de referencia P^* y Q^* requieren del cálculos de los valores de p_{loss} y Q_{vr} , que son respectivamente, la potencia activa instantánea necesaria para ajustar el voltaje del capacitor de dc -link a su valor de referencia, debido a las variaciones del voltaje en los mismos durante el funcionamiento del SAPF, y la potencia reactiva instantánea necesaria para ajustar el voltaje de la red ac a su valor de referencia. Además, para la determinación de las potencias de referencia, se utilizan las potencias P_L y Q_L activa y reactiva de la carga cuyas magnitudes se determinan mediante el uso de la transformación de Clarke.

El método de control basado en el esquema IRPT puede modificarse fácilmente para el control de las corrientes de red de forma indirecta. Para este caso, el modo de operación de corrección del factor de potencia del SAPF, se requiere que $P^* = P_L + p_{loss}$ y $Q^* = Q_L + Q_{vr} = 0$ en (2.8), y después de la transformación desde el marco de referencia $\alpha - \beta$ al marco de referencia en el dominio del tiempo $a-b-c$, las corrientes trifásicas transformadas son las corrientes de referencia de la red eléctrica y deben ser comparadas con las corrientes de red medidas como se muestra en la **Figura 2.8** para el control de corriente indirecta del SAPF.

2.7.3. Generación de referencia aplicado al SAPF basado en la teoría SRF

El esquema de control basada en la teoría SRF, propuesto por Robert H. Park en 1929 [109], utiliza las mediciones de corrientes trifásicas de la carga y con un lazo de seguimiento de fase (PLL) obtener el ángulo de fase θ de las corrientes de la red eléctrica, para luego aplicar la transformada de Park y trabajar en el SRF en coordenadas dq . En el SRF, la parte ac de la componente d representa las componentes armónicas de la corriente de carga, el cual pasa por un LPF de tal manera a obtener la componente ac y luego se adiciona las pérdidas de corriente provenientes del control PI del dc -link. Luego, se aplica nuevamente la transformada inversa de Park y se obtienen las corrientes de referencia como se muestra en la **Figura 2.9**

El PLL trifásico se utiliza para sincronizar las señales con los voltajes de red eléctrica. Las componentes de corriente $d-q$ pasan a través del LPF para extraer los componentes de

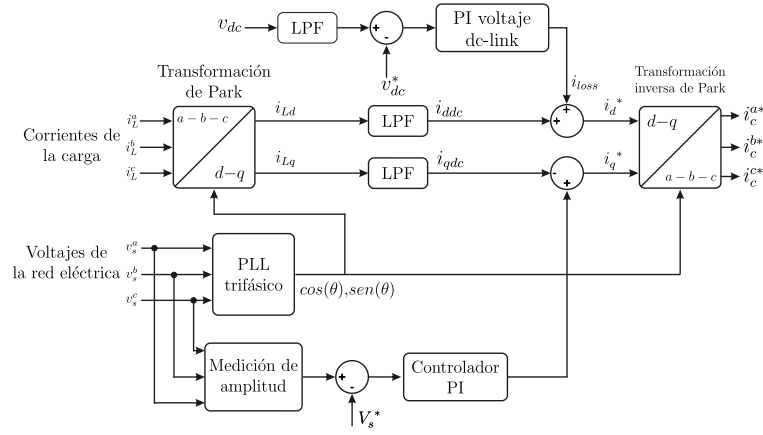


Figura 2.9 Generación de referencia del SAPF utilizando la teoría SRF.

dc de i_{Ld} e i_{Lq} . Las corrientes en los ejes $d - q$ pueden ser representadas como la suma de su componentes fundamentales y armónicos mediante 2.10:

$$\begin{bmatrix} i_{Ld} \\ i_{Lq} \\ i_{L0} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos\theta & -\sin\theta & \frac{1}{2} \\ \cos(\theta - \frac{2}{3}\pi) & -\sin(\theta - \frac{2}{3}\pi) & \frac{1}{2} \\ \cos(\theta + \frac{2}{3}\pi) & -\sin(\theta + \frac{2}{3}\pi) & \frac{1}{2} \end{bmatrix} \begin{bmatrix} i_L^a \\ i_L^b \\ i_L^c \end{bmatrix} \quad (2.9)$$

$$\begin{aligned} i_{Ld} &= i_{ddc} + i_{dac} \\ i_{Lq} &= i_{qdc} + i_{qac} \end{aligned} \quad (2.10)$$

La característica fundamental de este controlador es la utilización de un marco de referencia que gira en el plano complejo sincronizado con la señal de voltaje en el punto de conexión. La introducción de esta nueva transformación hace posible el cálculo de las componentes activa y no activa de la corriente de carga sin necesidad de determinar previamente la potencia. Un controlador SRF extrae las magnitudes de dc mediante un LPF y, por lo tanto, y una vez obtenida ésta, es posible calcular la componente ac , restando de la corriente ya sea i_{Ld} o i_{Lq} . El beneficio obtenido de la aplicación de la teoría SRF es que se trata con magnitudes de dc . Para aplicaciones de control, las magnitudes dc son fácilmente controlables sin presentar errores de estado estacionario.

La corriente de referencia de la red debe estar en fase con el voltaje de la red, pero sin componente de secuencia cero. Por lo tanto, se obtiene mediante la transformación inversa de Park y las consideraciones mencionadas las corrientes de referencia de la red como:

$$\begin{bmatrix} i_c^{a*} \\ i_c^{b*} \\ i_c^{c*} \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta & 1 \\ \cos\left(\theta - \frac{2}{3}\pi\right) & \sin\left(\theta - \frac{2}{3}\pi\right) & 1 \\ \cos\left(\theta + \frac{2}{3}\pi\right) & \sin\left(\theta + \frac{2}{3}\pi\right) & 1 \end{bmatrix} \begin{bmatrix} i_d^* \\ i_q^* \\ i_0^* \end{bmatrix} \quad (2.11)$$

2.8. Conclusiones del capítulo

El presente capítulo se han detallado las taxonomías del APF y sus aplicaciones en la red de distribución eléctrica. Se han detallado las principales topologías de convertidores utilizadas en el SAPF, así como el modelo matemático del SAPF y las principales estrategias de control aplicado al SAPF enfatizando el control predictivo MPC como estrategia a utilizar por sus principales ventajas tales como su baja complejidad sin necesidad de uso del modulador, posibilidad de múltiples objetivos a la vez con una sola ley de control, las restricciones del sistema están incluidas, la estrategia de control MPC aplicadas en sistemas de conversión de energía basado en convertidores de potencia tiene estados finitos de conmutación.

CAPÍTULO 3

ANÁLISIS TEÓRICO

3.1. Introducción

En los últimos años, los temas de calidad y eficiencia de energética se han consolidado como un tema científico en el campo de la ingeniería eléctrica debido a los requisitos técnicos para la conexión a la red eléctrica. En realidad, el factor de potencia (FP), sobrevoltajes, el desequilibrio de carga, los excesivos armónicos de corriente, los transitorios y las oscilaciones han sido una preocupación importante en los sistemas de transmisión y distribución de energía eléctrica [110], [111]. Las cargas no lineales normalmente producen perturbaciones en los sistemas de transmisión y distribución de energía, provocando una distorsión armónica de alto nivel en las corrientes y voltajes de fase. Además, las cargas no lineales distorsionan la corriente de la red eléctrica, lo que provoca un THD excesivo que restringe la transferencia de potencia activa máxima, lo que agrega pérdidas a los sistemas de transmisión y distribución de energía que afectan su estabilidad y confiabilidad [112], [113].

Hoy en día, varios desarrollos de transmisión y distribución de CA flexible y sus controladores, como los SAPF, se han implementado con éxito para superar los inconvenientes antes mencionados. Recientemente, los convertidores multinivel se han convertido en una alternativa popular para superar las restricciones tecnológicas de los dispositivos semiconductores que tienen potencia limitadas [86], [114]. Entre todas las topologías multinivel, el convertidor CHB es una de las configuraciones utilizadas como SAPF, especialmente útil para la compensación de armónicos de corriente [115], [116]. Los sistemas SAPF basados en convertidores CHB se han utilizado ampliamente en aplicaciones de alta potencia debido a sus ventajas inherentes, tales como: pérdidas de conmutación reducidas, mayor eficiencia de conversión, estructura modular, escalabilidad para extenderse a más niveles y mayor número de estados de conmutación redundantes [117], [118]. Comúnmente, el convertidor multinivel SAPF basado en CHB ha sido diseñado utilizando dispositivos eléctricos de potencia IGBT. Pero, recientemente, los dispositivos SiC-MOSFET han llamado la atención de los investigadores porque éstos dispositivos pueden alcanzar altas frecuencias de conmutación, mucho más altas de lo que podría lograrse con un convertidor multinivel basado en IGBTs [119], [120].

Las estrategias de control implementadas en el SAPF son las técnicas de control PID que necesitan una gran cantidad de variables a medir, el control de histéresis, que tiene un ancho de banda alto, produciendo la mayor propagación de distorsión armónica de bajo orden y un bajo valor, aumentando las pérdidas de conmutación. Por otro lado, el MPC es una técnica de control no lineal aplicada a los convertidores de potencia, que tiene algunas ventajas como una rápida respuesta dinámica, la capacidad de manejar sistemas multivariables, no linealidades y restricciones [121], [122]. Algunas desventajas son que depende del modelo del sistema y utiliza una frecuencia de conmutación variable, lo que provoca la propagación de armónicos de bajo orden en la corriente de salida que deterioran el rendimiento del sistema [123], [124]. Por otro lado, el MPC aplicado al SAPF basado en convertidores de puente-H en cascada de siete niveles utiliza los estados de conmutación, que corresponden a un nivel de voltaje específico, que normalmente es un voltaje de referencia constante, pero que tiene capacitores flotantes tales como el *dc-link*, mediante el cual se cargan y descargan según la polaridad de la corriente del filtro, lo que genera ondulaciones de voltaje de los condensadores [125], [48]. Por lo tanto, existe una propagación del error entre los voltajes de *dc-link* medidas con respecto a su valor de referencia [126], [127].

En este capítulo se presenta la implementación de una estrategia de modulación que combina el espacio vectorial, la modulación por desplazamiento de fase (SV-PSPWM) y la estrategia de MPC aplicada al SAPF basado en convertidores CHB de 7 niveles [128],

[129]. Por otro lado, la estrategia de control propuesta combina una solución subóptima para lograr el equilibrio de voltaje del *dc*-link, simplificando la estructura de control [130].

3.1.1. Modelo predictivo SAPF basado en convertidor CHB

El modelo predictivo se puede obtener a partir de (2.1) utilizando un método de discretización de Euler en adelante. El método de Euler es el método explícito más básico para la integración numérica de ecuaciones diferenciales ordinarias y, en consecuencia, conlleva una carga computacional baja, lo que beneficia la implementación experimental. El modelo de tiempo discreto SAPF está dado por:

$$i_c^\phi(k+1) = \left(1 - \frac{R_f T_s}{L_f}\right) i_c^\phi(k) + \frac{T_s}{L_f} (v_c^\phi(k) - v_s^\phi(k)) \quad (3.1)$$

donde k representa el instante de muestreo de tiempo discreto real, T_s es el tiempo de muestreo e $i_c^\phi(k+1)$ es la predicción de corrientes de fase SAPF realizadas en la muestra $k+1$. Además, en (3.1), $i_c^\phi(k)$ corresponde a la corriente medida en el filtro de salida en el tiempo de muestreo actual k . Mientras que $v_s^\phi(k)$ corresponde al voltaje de fase medida en la red eléctrica en el mismo tiempo de muestreo k . Luego, éstos valores medidos son utilizados por el control predictivo de corriente. Por último, $v_c^\phi(k)$ se calcula en cada instante de muestreo utilizando el modelo discreto del sistema de tiempo discreto en (3.1) y usa los voltajes medidos del capacitor de *dc*-link $v_{dc1}^\phi(k)$, $v_{dc2}^\phi(k)$ y $v_{dc3}^\phi(k)$, en donde los índices (1, 2 y 3) representan las celdas de CHB por fase.

Debido a la topología CHB que utiliza *dc*-link independiente mediante condensadores en combinación con las señales de activación, se obtiene el modelo de los voltajes de salida del convertidor:

$$v_c^\phi(k) = (Sf_{11}^\phi - Sf_{12}^\phi) v_{dc1}^\phi(k) + (Sf_{21}^\phi - Sf_{22}^\phi) v_{dc2}^\phi(k) + (Sf_{31}^\phi - Sf_{32}^\phi) v_{dc3}^\phi(k) \quad (3.2)$$

A partir de esto se obtiene el modelo de control, evitando utilizar un voltaje de referencia fijo. En cambio, los voltajes medidos de cada convertidor con su signo correspondiente se utilizan para obtener las salidas de voltaje reales del convertidor en combinación con los estados de conmutación que se muestra en la **Tabla 3.1**.

Tabla 3.1 Niveles de voltaje a la salida del SAPF.

Sf_{11}^ϕ	Sf_{12}^ϕ	Sf_{21}^ϕ	Sf_{22}^ϕ	Sf_{31}^ϕ	Sf_{32}^ϕ	v_c^ϕ
0	1	0	1	0	1	$-3v_{dc}$
0	0	0	1	0	1	$-2v_{dc}$
0	0	0	0	0	1	$-v_{dc}$
0	0	0	0	0	0	0
0	0	0	0	1	0	$+v_{dc}$
0	0	1	0	1	0	$+2v_{dc}$
1	0	1	0	1	0	$+3v_{dc}$

3.2. Generación de la corriente de referencia de compensación IRPT

Las referencias de potencia instantánea activa y reactiva se obtienen mediante la transformación de Clarke en el marco de referencia $\alpha - \beta$. Con el propósito de obtener una expresión $\alpha - \beta$ basado en el criterio invariante en potencia, se utiliza la siguiente matriz de transformación:

$$\mathbf{T} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \quad (3.3)$$

Aplicando (3.3) los voltajes de la red eléctrica $v_s^\phi(k)$ y las corrientes de fase en la carga $i_L^\phi(k)$, en el marco de referencia $\alpha - \beta$ resultan:

$$\begin{bmatrix} v_s^\alpha(k) \\ v_s^\beta(k) \end{bmatrix} = \mathbf{T} \begin{bmatrix} v_s^a(k) \\ v_s^b(k) \\ v_s^c(k) \end{bmatrix} \quad (3.4)$$

$$\begin{bmatrix} i_L^\alpha(k) \\ i_L^\beta(k) \end{bmatrix} = \mathbf{T} \begin{bmatrix} i_L^a(k) \\ i_L^b(k) \\ i_L^c(k) \end{bmatrix} \quad (3.5)$$

En consecuencia, las potencias instantáneas activa y reactiva consumidas por la carga están dadas por las siguientes ecuaciones [78]:

$$P_L(k) = v_s^\alpha(k)i_L^\alpha(k) + v_s^\beta(k)i_L^\beta(k) \quad (3.6)$$

$$Q_L(k) = v_s^\beta(k)i_L^\alpha(k) - v_s^\alpha(k)i_L^\beta(k) \quad (3.7)$$

Con el fin de lograr un factor de potencia unitario en el lado de la red eléctrica y considerando que idealmente el filtro activo de potencia multinivel no absorbe potencia activa, las referencias de potencia instantáneas se pueden escribir como:

$$P_c^*(k) = 0 \quad (3.8)$$

$$Q_c^*(k) = Q_L(k) \quad (3.9)$$

donde el superíndice (*) denota las variables de referencia, Q_L es la potencia reactiva instantánea de la carga que debe ser compensada por el filtro activo de potencia y, $P_c^*(k)$ y $Q_c^*(k)$ son las referencias de potencia instantánea activa y reactiva, respectivamente. Por otro lado, las referencias de potencia activa y reactiva pueden ser expresadas en términos de corrientes de referencia en el marco de referencia $\alpha - \beta$, según las siguientes ecuaciones:

$$\begin{bmatrix} i_c^{\alpha*}(k) \\ i_c^{\beta*}(k) \end{bmatrix} = \frac{1}{v_s^\alpha(k)^2 + v_s^\beta(k)^2} \begin{bmatrix} v_s^\alpha(k) & v_s^\beta(k) \\ v_s^\beta(k) & -v_s^\alpha(k) \end{bmatrix} \begin{bmatrix} P_c^*(k) \\ Q_c^*(k) \end{bmatrix} \quad (3.10)$$

Finalmente, las referencias de corrientes de fase del filtro activo de potencia multinivel utilizadas en el proceso de optimización son:

$$\begin{bmatrix} i_c^{a*}(k) \\ i_c^{b*}(k) \\ i_c^{c*}(k) \end{bmatrix} = \mathbf{T}^{-1} \begin{bmatrix} i_c^{\alpha*}(k) \\ i_c^{\beta*}(k) \\ 0 \end{bmatrix} \quad (3.11)$$

3.3. Generación de la corriente de referencia de compensación SRF

La otra técnica utilizada en esta tesis para el calculo de las corrientes de referencia $i_c^{\phi*}$ se basa en la técnica SRF. En la **Figura 3.1** a la izquierda muestra el procedimiento detallado en donde primeramente se obtiene el ángulo θ de la red eléctrica a través de un PLL. Este ángulo se usa para transformar del plano $a - b - c$ al plano $d - q - 0$ y viceversa. Luego, se utiliza un filtro de paso bajo (LPF) para eliminar el componente de ca de la corriente de medición de carga I_{Ld} (componente d) [131].

$$\begin{bmatrix} i_{Lq} \\ i_{Ld} \\ i_{L0} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos\theta & \cos(\theta - \frac{2}{3}\pi) & \cos(\theta + \frac{2}{3}\pi) \\ \sin\theta & \sin(\theta - \frac{2}{3}\pi) & \sin(\theta + \frac{2}{3}\pi) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} i_L^a \\ i_L^b \\ i_L^c \end{bmatrix}. \quad (3.12)$$

Una vez obtenidas las componentes i_{Ld} y i_{Lq} de la corriente de carga, se aplica un filtro paso bajo de tal manera a obtener la componente continua $\bar{i}_{Lddc}$.

Antes de la operación del SAPF, todos los capacitores deben cargarse al voltaje de referencia v_{dc}^* . El SAPF, durante su funcionamiento, puede absorber o inyectar corriente a la red eléctrica. Este último produce la carga y descarga de los capacitores C_{dcx}^ϕ de cada CHB. En consecuencia, provoca el desbalance de los voltajes del dc -link [132]. Para resolver este problema, se usa un controlador que proporciona el valor de la pérdida de corriente i_{loss} de los capacitores que se absorbe de la red eléctrica. Por lo tanto, la corriente de pérdida representa las corrientes de consumo en cada fase de los condensadores C_{dcx}^ϕ , y el control PI está siendo utilizado para compensar esta pérdida de tal manera que equilibre el voltaje del dc -link v_{dcx}^ϕ . Las ecuaciones correspondientes al control PI en tiempo discreto se muestran a continuación:

$$e^\phi(k) = v_{dc}^*(k) - v_{dc1}^\phi(k) \quad (3.13)$$

$$i_{loss}^\phi = i_{loss}^\phi(k-1) + kp (e^\phi(k) - e^\phi(k-1)) + T_{PI} ki e^\phi(k) \quad (3.14)$$

$$i_{loss} = \frac{1}{3} \sum_{\phi=a,b,c} i_{loss}^\phi \quad (3.15)$$

donde $e^\phi(k)$ representa el error entre la referencia y los voltajes medidos previamente filtrados v_{dc1}^ϕ . Luego, se calcula la corriente de pérdida i_{loss}^ϕ , siendo $i_{loss}^\phi(k-1)$ la corriente de pérdida estimada en el instante anterior, $e(k-1)$ el error de voltaje calculado en el último instante, T_{PI} representa el tiempo de actuación del controlador PI y finalmente i_{loss} que representa el promedio de las corrientes de pérdida de cada fase.

Finalmente las componentes i_{cd}^* e i_{cq}^* de referencia es:

$$\begin{aligned} i_{cd}^*(k) &= i_{Ld} - i_{Lddc} - i_{loss} \\ i_{cq}^*(k) &= i_{Lq}. \end{aligned} \quad (3.16)$$

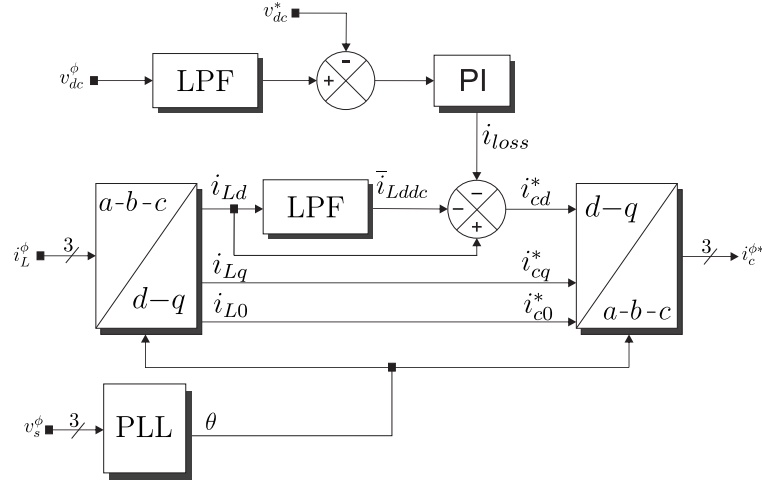


Figura 3.1 Generación de referencia SRF aplicado al SAPF trifásico basado en CHB de 7 niveles.

Luego, dado que se obtiene la referencia en d componente de la referencia actual, se aplica la transformación inversa de Park para encontrar las corrientes de referencia $i_c^{\phi*}$ a utilizar por el controlador MPC propuesto.

$$\begin{bmatrix} i_c^{\alpha*}(k) \\ i_c^{\beta*}(k) \end{bmatrix} = \begin{bmatrix} \sin\theta & \cos\theta \\ -\cos\theta & \sin\theta \end{bmatrix} \begin{bmatrix} i_{cd}^*(k) \\ i_{cq}^*(k) \end{bmatrix} \quad (3.17)$$

$$\begin{bmatrix} i_c^{a*}(k) \\ i_c^{b*}(k) \\ i_c^{c*}(k) \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_c^{\alpha*}(k) \\ i_c^{\beta*}(k) \end{bmatrix} \quad (3.18)$$

3.3.1. Proceso de optimización

En la técnica MPC, se calcula una función de costo para diferentes condiciones de estado de conmutación de un sistema bajo estudio para encontrar el vector de voltaje más adecuado. En otras palabras, para todas las condiciones de estado de conmutación factibles, se calcula la función de costo y, a continuación, se selecciona la que minimiza la función de costo predefinida y se aplica durante el siguiente tiempo de muestreo al sistema [133]. En esta tesis, la función de costo se define como el error entre la predicción y la referencia. En el esquema de control trifásico, las funciones de costo se evalúan independientemente de las siguientes ecuaciones:

$$g^\phi = \| i_c^{\phi*} - \hat{i}_c^\phi(k+1) \|^2 \quad (3.19)$$

A continuación, el algoritmo de optimización selecciona el vector óptimo $S_{\eta,opt}^\phi$ que corresponde al voltaje que minimiza la función de costo, para luego enviarlo a la etapa moduladora.

3.4. La modulación Phase-Shift Space Vector PWM

Como se mencionó en la sección anterior, el algoritmo de optimización evalúa todos los estados de conmutación factibles. En la **Tabla 3.2**, se muestra los estados de conmutación para una fase del SAPF basado en convertidores CHB de 7 niveles, se tiene $n = 64$ estados de voltajes posibles para una fase.

Tabla 3.2: Estados de conmutación del convertidor CHB de 7 niveles.

$S_{x,y}$						n	v_c^ϕ
Celda 1		Celda 2		Celda 3			
S_{11}	S_{13}	S_{21}	S_{23}	S_{31}	S_{33}		
0	0	0	0	0	0	1	0
0	0	0	0	0	1	2	-1
0	0	0	0	1	0	3	1
0	0	0	0	1	1	4	0
0	0	0	1	0	0	5	-1
0	0	0	1	0	1	6	-2
0	0	0	1	1	0	7	0
0	0	0	1	1	1	8	-1
0	0	1	0	0	0	9	1
0	0	1	0	0	1	10	0
0	0	1	0	1	0	11	2
0	0	1	0	1	1	12	1
0	0	1	1	0	0	13	0

Sigue en la página siguiente.

Tabla 3.2: Estados de conmutación del convertidor CHB de 7 niveles.
(Continuación).

$S_{x,y}$						n	v_c^ϕ
Celda 1		Celda 2		Celda 3			
S_{11}	S_{13}	S_{21}	S_{23}	S_{31}	S_{33}		
0	0	1	1	0	1	14	-1
0	0	1	1	1	0	15	1
0	0	1	1	1	1	16	0
0	1	0	0	0	0	17	-1
0	1	0	0	0	1	18	-2
0	1	0	0	1	0	19	0
0	1	0	0	1	1	20	-1
0	1	0	1	0	0	21	-2
0	1	0	1	0	1	22	-3
0	1	0	1	1	0	23	-1
0	1	0	1	1	1	24	-2
0	1	1	0	0	0	25	0
0	1	1	0	0	1	26	-1
0	1	1	0	1	0	27	1
0	1	1	0	1	1	28	0
0	1	1	1	0	0	29	-1
0	1	1	1	0	1	30	-2
0	1	1	1	1	0	31	0
0	1	1	1	1	1	32	-1
1	0	0	0	0	0	33	1
1	0	0	0	0	1	34	0
1	0	0	0	1	0	35	2
1	0	0	0	1	1	36	1
1	0	0	1	0	0	37	0

Sigue en la página siguiente.

Tabla 3.2: Estados de conmutación del convertidor CHB de 7 niveles.
(Continuación).

$S_{x,y}$						n	v_c^ϕ
Celda 1		Celda 2		Celda 3			
S_{11}	S_{13}	S_{21}	S_{23}	S_{31}	S_{33}		
1	0	0	1	0	1	38	-1
1	0	0	1	1	0	39	1
1	0	0	1	1	1	40	0
1	0	1	0	0	0	41	2
1	0	1	0	0	1	42	1
1	0	1	0	1	0	43	3
1	0	1	0	1	1	44	2
1	0	1	1	0	0	45	1
1	0	1	1	0	1	46	0
1	0	1	1	1	0	47	2
1	0	1	1	1	1	48	1
1	1	0	0	0	0	49	0
1	1	0	0	0	1	50	-1
1	1	0	0	1	0	51	1
1	1	0	0	1	1	52	0
1	1	0	1	0	0	53	-1
1	1	0	1	0	1	54	-2
1	1	0	1	1	0	55	0
1	1	0	1	1	1	56	-1
1	1	1	0	0	0	57	1
1	1	1	0	0	1	58	0
1	1	1	0	1	0	59	2
1	1	1	0	1	1	60	1
1	1	1	1	0	0	61	0

Sigue en la página siguiente.

Tabla 3.2: Estados de conmutación del convertidor CHB de 7 niveles.
(Continuación).

$S_{x,y}$						n	v_c^ϕ
Celda 1		Celda 2		Celda 3			
S_{11}	S_{13}	S_{21}	S_{23}	S_{31}	S_{33}		
1	1	1	1	0	1	62	-1
1	1	1	1	1	0	63	1
1	1	1	1	1	1	64	0

Para obtener la cantidad de vectores de voltaje en el espacio vectorial, se combina con los demás estados de conmutación de las otras dos fases, por lo tanto, la cantidad de vectores de voltaje en el espacio vectorial sería $n \times n \times n = 64^3 = 262\,144$ vectores de voltajes para el SAPF basado en convertidores CHB de 7 niveles. Esto último conlleva una elevada carga computacional que imposibilita su implementación en los procesadores de señales digitales disponibles en la actualidad [134]. Por lo tanto, en esta tesis se propone una estructura de modulación que consiste en una combinación del espacio vectorial con modulación por desplazamiento de fase. El objetivo de este enfoque es reducir el costo computacional al reducir el número de vectores utilizando como base una topología CHB de 3 niveles correspondiente a un CHB por fase, donde los vectores se representan como el primer y segundo hexágono delineados como se muestra en la **Figura 3.2**, el tercer y cuarto hexágono representan el segundo nivel al agregar un CHB, el quinto y sexto hexágono definen el tercer nivel al agregar un tercer CHB [135].

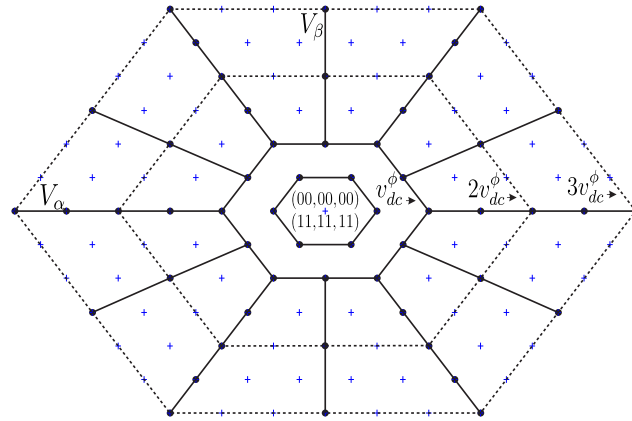


Figura 3.2 Diagrama del espacio vectorial del SAPF trifásico basado en CHB de 7 niveles.

Tabla 3.3 Estados de voltaje trifásico en el espacio vectorial.

v_c^a	v_c^b	v_c^c	η
0	-1	-1	1
1	1	0	2
-1	0	-1	3
0	1	1	4
-1	-1	0	5
1	0	1	6
1	-1	-1	7
1	0	-1	8
1	1	-1	9
0	1	-1	10
-1	1	-1	11
-1	1	0	12
-1	1	1	13
-1	0	1	14
-1	-1	1	15
.	.	.	.
.	.	.	.
3	-3	0	54

Para reducir el número de vectores, los vectores de primer nivel se extrapolan al segundo y tercer nivel. Por ejemplo, si los estados de conmutación óptimos corresponden al primer nivel son (1 0 1) para seleccionar los vectores de voltaje óptimos correspondientes al segundo nivel es (2 0 2), se realiza el mismo análisis para los vectores de voltaje correspondientes al tercer nivel, en la **Tabla 3.3** se muestra los estados de voltaje en el espacio vectorial. Esta propuesta reduce significativamente las interacciones de 262 144 a 54 un 99.97 % correspondientes al número de puntos del diagrama en espacio vectorial y por lo tanto reduce el costo computacional y posibilita la implementación en tiempo real [136].

Una vez seleccionado el nivel de voltaje óptimo se realiza el PSPWM que consta de tres portadoras triangulares $\frac{180^\circ}{3}$ desfasadas entre sí y con la misma frecuencia para obtener los tiempos de activación de las señales de disparo.

$$v_{ct}^\phi = \frac{v_{c,\eta,opt}^\phi}{3} \quad (3.20)$$

donde v_{ct}^ϕ es un modulador normalizado entre -1 y 1 , y $v_{c,\eta,opt}^\phi$ son los niveles de voltaje óptimos seleccionados en el espacio vectorial. El Algoritmo resume el proceso de optimización.

Algoritmo de optimización del controlador de corriente MPC modulado propuesto.

1. Inicio $g_{opt}^a := \infty, g_{opt}^b := \infty, g_{opt}^c := \infty, \eta := 0$. Ec. (3.19)
 2. Cálculo de corrientes de referencia. Ec. (3.11) o Ec. (3.18)
 3. **while** $\eta \leq \varepsilon$ **do**
 4. $S_\eta^\phi \leftarrow S_{xy}^\phi \forall x \ \& \ y = 1, 2, 3$
 5. Cálculo de las predicciones de corrientes
 6. Cálculo de la función de costo
 7. **if** $g^a < g_{opt}^a$ **then**
 8. $g_{opt}^a \leftarrow g^a, S_{opt}^a \leftarrow S_\eta^a$
 9. **end if**
 10. **if** $g^b < g_{opt}^b$ **then**
 11. $g_{opt}^b \leftarrow g^b, S_{opt}^b \leftarrow S_\eta^b$
 12. **end if**
 13. **if** $g^c < g_{opt}^c$ **then**
 14. $g_{opt}^c \leftarrow g^c, S_{opt}^c \leftarrow S_\eta^c$
 15. **end if**
 16. $\eta := \eta + 1$
 17. **end while**
 18. Cálculo de las señales de modulación
 19. Se obtienen las señales de disparo
 20. Se aplica las señales de disparo.
-

3.5. Análisis teórico mediante simulación

A continuación se presentan los resultados teóricos mediante simulación utilizando la herramienta computacional Matlab/Simulink. Los resultados de simulación se obtuvieron utilizando los parámetros de una plataforma experimental como se muestra en la **Tabla 3.4** y aplicando la estrategia de control MPC con la modulación SV-PSPWM al SAPF trifásico de 7 niveles. A continuación se presenta la estrategia de control con las dos principales esquemas para la obtención de la referencia la teoría IRPT y la teoría de SRF. Para el análisis de los resultados se utilizaron el MSE y el THD como parámetros de calidad de la energía.

$$\text{MSE}(\Psi) = \sqrt{\frac{1}{N} \sum_{j=1}^N \Psi_j^2} \quad (3.21)$$

Tabla 3.4 Parámetros eléctricos utilizados en las simulaciones.

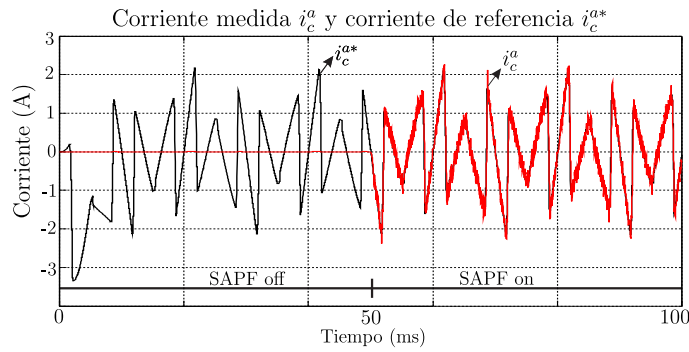
Parámetro	Símbolo	Valor	Unidad
Tiempo de muestreo	T_s	50	μs
Paso de simulación	T_m	2	μs
Tiempo de interconexión	t_{on}	50	ms
Resistencia de la carga	R_L	75	Ω
Inductancia de la carga	L_L	1	mH
Resistencia del filtro	R_c	0.35	Ω
Inductancia del filtro	L_c	10	mH
Voltaje de bus continua	dc -link	85	V
Capacitancia del bus de continua	C_{dc}	23420	μF
Frecuencia de la red	f_e	50	Hz
Voltaje de la red	v_s	120	V

$$THD = \sqrt{\frac{1}{i_1^2} \sum_{i=2}^N i_i^2} \quad (3.22)$$

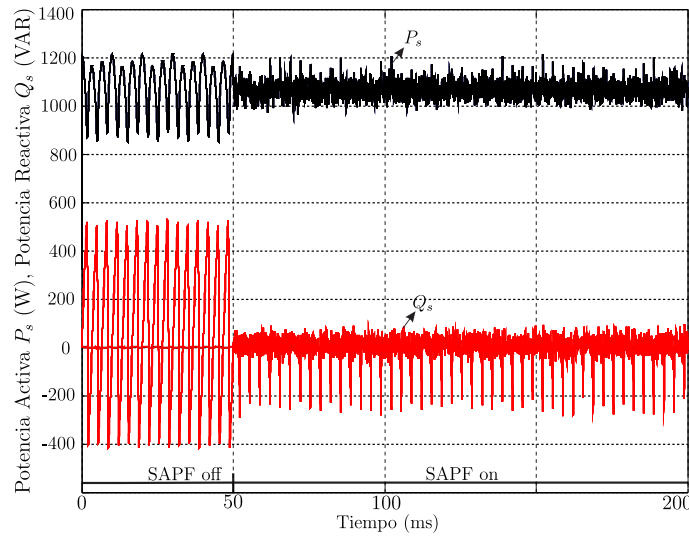
3.5.1. Resultados del SAPF basado en la estrategia IRPT

Primeramente se presenta los resultados del control MPC con modulación SV-PSPWM utilizando la teoría de potencia instantánea. En la **Figura 3.3 (a)** se presenta la respuesta transitoria y seguimiento de la corriente medida i_c^a y la corriente de referencia i_c^{a*} a la salida del SAPF correspondiente a la fase a . Primeramente el SAPF se encuentra inactivo hasta los 50ms, una vez activo el SAPF, se observa el seguimiento de la corriente medida con una amplitud pico de 2 A y presenta un MSE de 0.1475 A.

En la **Figura 3.3 (b)** se presenta la respuesta transitoria de la compensación de los armónicos representados en potencia activa P_s y potencia reactiva Q_s de la red eléctrica. La carga no lineal consume una Potencia Activa de $P_s=1200$ W de amplitud pico y una potencia reactiva de $Q_s= 500$ VAR de amplitud pico. Inicialmente el SAPF se encuentra inactivo y se activa a los 50 ms, una vez conectado el SAPF se realiza la compensación de armónicos de corriente, el cual repercute en la compensación de las oscilaciones de potencia activa, manteniendo su parte dc y la compensación de las oscilaciones en potencia reactiva aproximadamente en un valor de 50 VAR que representa una compensación del 90 %.



(a) Seguimiento de la corriente medida i_c^a y la corriente de referencia i_c^{a*} en IRPT.



(b) Compensación de armónicos de la red eléctrica en el IRPT.

Figura 3.3 Seguimiento de corriente del SAPF y compensación de potencia reactiva en IRPT.

En la **Figura 3.4** se presenta la compensación de los armónicos de corriente de la red eléctrica en la fase a . En la **Figura 3.4 (a)** se presenta el análisis de THD de la corriente de carga i_L^a , con un THD del 28.6 %. En la **Figura 3.4 (b)** se presenta el análisis de THD de la corriente de la red eléctrica i_s^a una vez conectado el SAPF, con un THD del 6.59 %, el cual representa una compensación del 77 %.

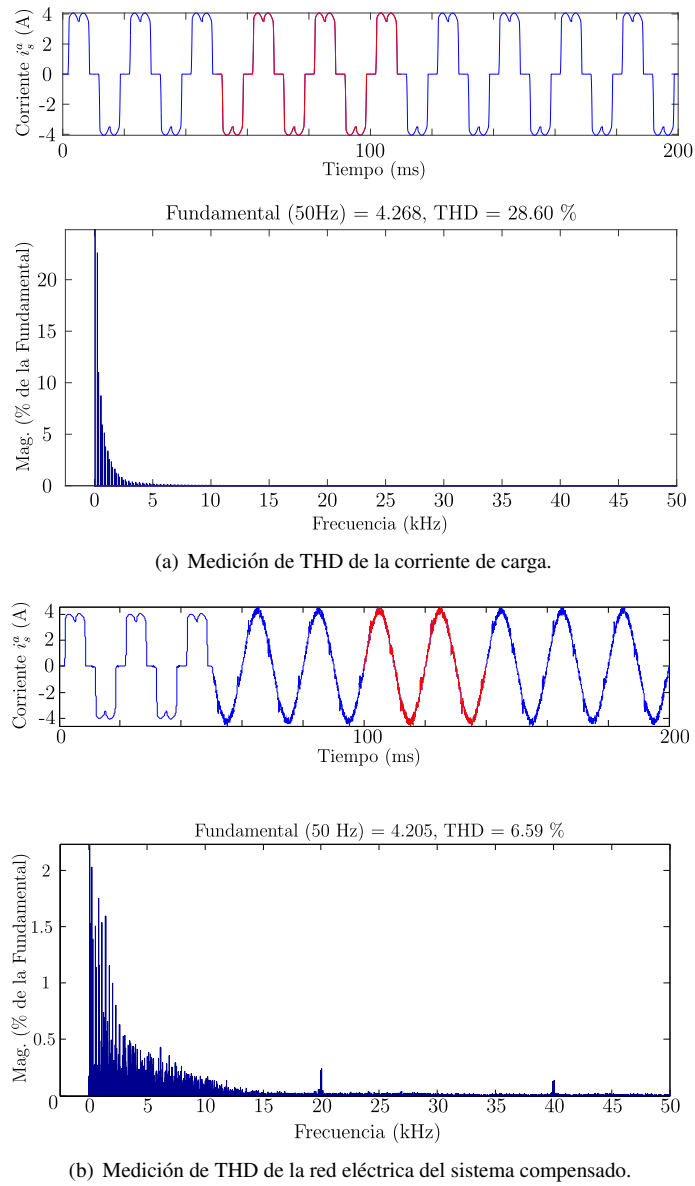
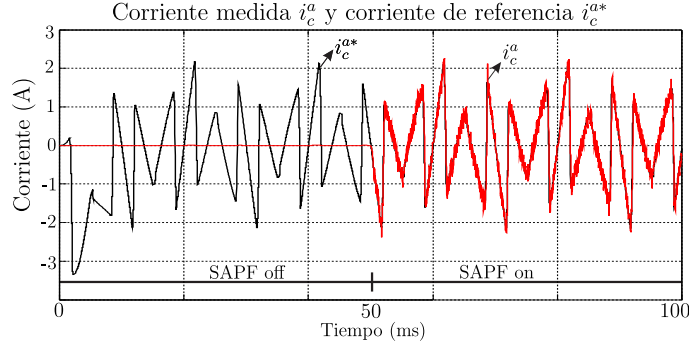


Figura 3.4 Análisis de THD de la corriente de la red eléctrica en IRPT.

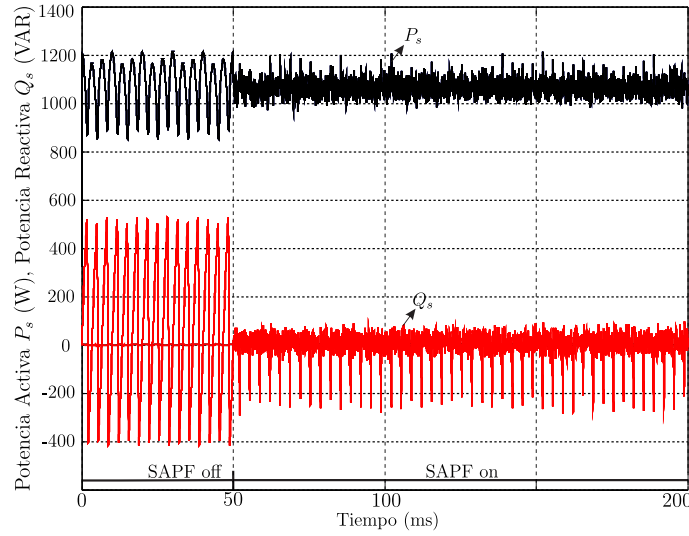
3.5.2. Resultados del SAPF basado en la estrategia SRF

Análogamente a las pruebas llevadas a cabo en el apartado anterior, a continuación se evalúa el desempeño del controlador propuesto pero utilizando la técnica SRF.

En la **Figura 3.5 (a)**, se presenta la respuesta transitoria del seguimiento de la corriente medida i_c^a y la corriente de referencia i_c^{a*} a la salida del SAPF correspondiente a la fase a . Primeramente el SAPF se encuentra inactivo hasta los 40ms, una vez activo el SAPF, se observa el seguimiento de la corriente medida con una amplitud pico de 2 A y presenta un MSE de 0.113 A.



(a) Seguimiento de la corriente medida i_c^a y corriente de referencia i_c^{a*} en SRF.



(b) Compensación de armónicos de la red eléctrica en el SRF.

Figura 3.5 Respuesta transitoria de la corriente del SAPF y la potencia activa y reactiva en SRF.

En la **Figura 3.5 (b)** se presenta la respuesta transitoria de la compensación de los armónicos representados en potencia activa P_s y potencia reactiva Q_s de la red eléctrica. La carga no lineal consume una Potencia Activa de $P_s=1200$ W de amplitud pico y una potencia reactiva de $Q_s= 500$ VAR de amplitud pico. Inicialmente el SAPF se encuentra

inactivo y se activa a los 40 ms, una vez conectado el SAPF se realiza la compensación de armónicos de corriente, el cual repercute en la compensación de las oscilaciones de potencia activa, manteniendo su parte dc y la compensación de las oscilaciones en potencia reactiva aproximadamente en un valor de 50 VAR que representa una compensación del 90 %.

En la **Figura 3.4** (a) se muestran los resultados experimentales obtenidos para una carga $R_L = 72 \Omega$, la imagen corresponde a la medición de la corriente de red distorsionada, antes de la puesta en marcha del SAPF, en la misma se observa un nivel de THD de 28,6 %. La **Figura 3.6** (b) muestra la medición del nivel de THD de la corriente de red compensada, en la misma se observa un THD de 5,1 %, en base a estas mediciones se observa una reducción significativa en el nivel de THD en la corriente de la red eléctrica.

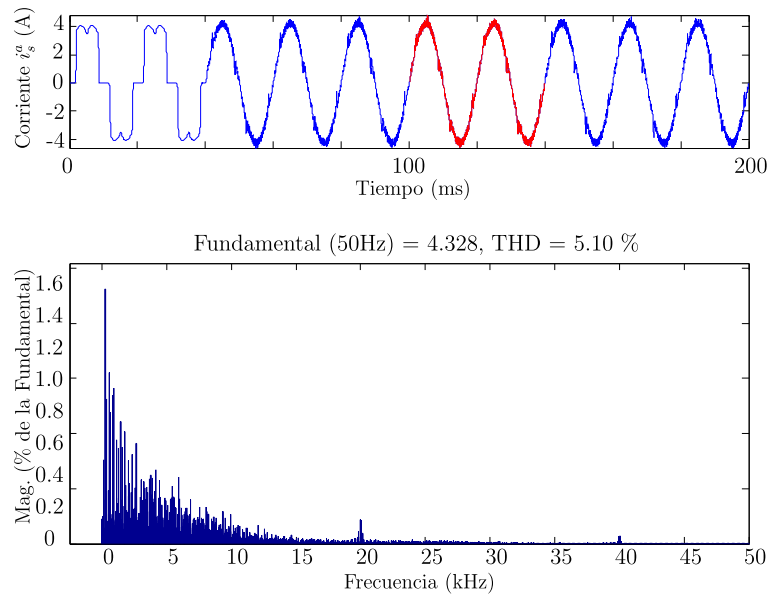


Figura 3.6 Compensación de armónicos de corriente i_s^a de la red eléctrica.

3.6. Conclusiones del capítulo

En el presente capítulo se ha abordado el análisis teórico mediante resultados de simulación, utilizando la herramienta computacional Matlab/Simulink. Se ha analizado los resultados de simulación la estrategia de control MPC con modulación SV-PSPWM propuesta, utilizando los dos esquemas de generación de referencia IRPT y SRF. Ambos esquemas fueron evaluados mediante los parámetros de calidad de energía MSE y la THD, obteniendo los siguientes resultados, para el esquema IRPT se obtuvieron valores de $MSE = 0.1475$ A y un $THD = 6.59$ %. Para el esquema SRF se obtuvieron valores de $MSE = 0.1130$ A y un $THD = 5.10$ %. Para la obtención de resultados experimentales se ha optado por el esquema SRF ya que ha presentado mejores resultados con una mejora del 1.49 %.

CAPÍTULO 4

VALIDACIÓN EXPERIMENTAL DEL CONTROL PREDICTIVO APLICADO AL SAPF

4.1. Introducción

En el presente capítulo se presenta los resultados experimentales de la estrategia de control propuesta aplicado al SAPF trifásico basados en convertidores CHB de 7 niveles. Primeramente se realiza una descripción de sistema en general, como la red eléctrica de distribución, la carga no lineal y la bancada experimental del SAPF con el controlador utilizado con las respectivas mediciones realizadas. Luego, se analiza los resultados obtenidos evaluando la compensación de potencia reactiva y armónicos de corriente en la red eléctrica, realizando mediciones de corriente y voltajes de la red eléctrica, el control, así como su plataforma de visualización temporal para el monitoreo y adquisición de datos, se implementa en el dispositivo dSPACE MicroLabBox.

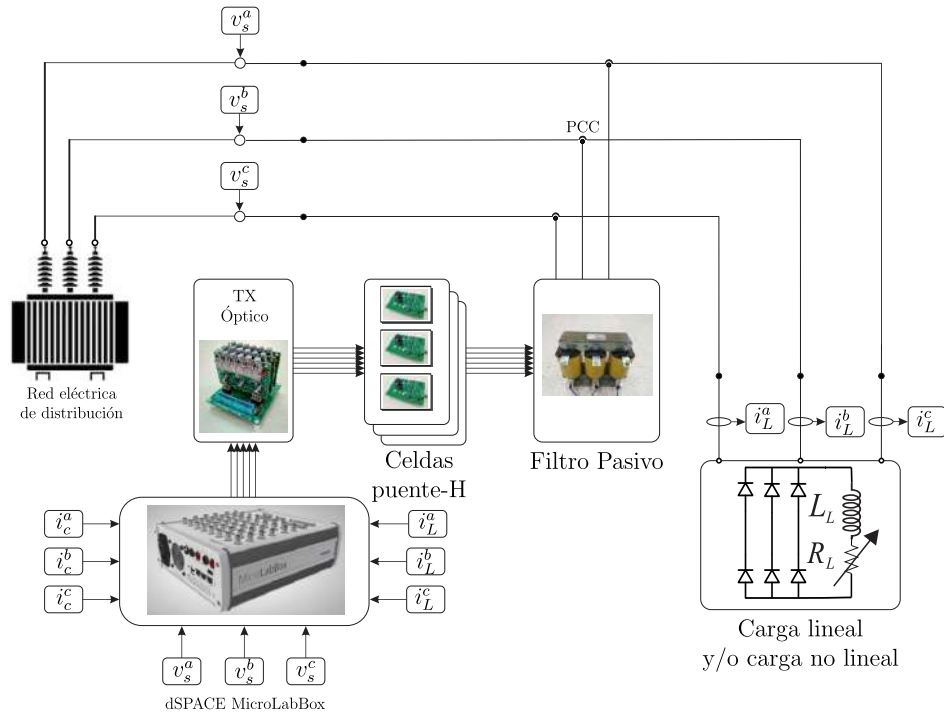


Figura 4.1 Esquema de la plataforma experimental.

4.2. Descripción del sistema

El esquema general propuesto a ser implementado para la validación experimental del SAPF, con cada uno de los bloques que lo componen se presenta en la **Figura 4.1**. La plataforma experimental consta de la red eléctrica de distribución trifásica conectado a un rectificador trifásico como carga no lineal, luego, conectada en el PCC se encuentra el SAPF que consta del controlador dSPACE MicroLabBox realizando las mediciones de la corriente de carga i_L^ϕ , de la corriente a la salida del SAPF i_c^ϕ y los voltajes de la red eléctrica v_s^ϕ . A la salida del controlador se tienen las 18 señales digitales de activación, que primeramente se acondicionan con un driver de fibra óptica para realizar las activaciones de los SiC-MOSFET de los 9 CHB, cada fase consta de 3 CHB conectados en serie para la generación de los 7 niveles voltajes a la salida del convertidor multinivel. Finalmente a la salida del convertidor multinivel se tiene una inductancia como filtro pasivo de tal manera a obtener una corriente adecuada a la salida del SAPF que es inyectada a la red eléctrica en el punto PCC.

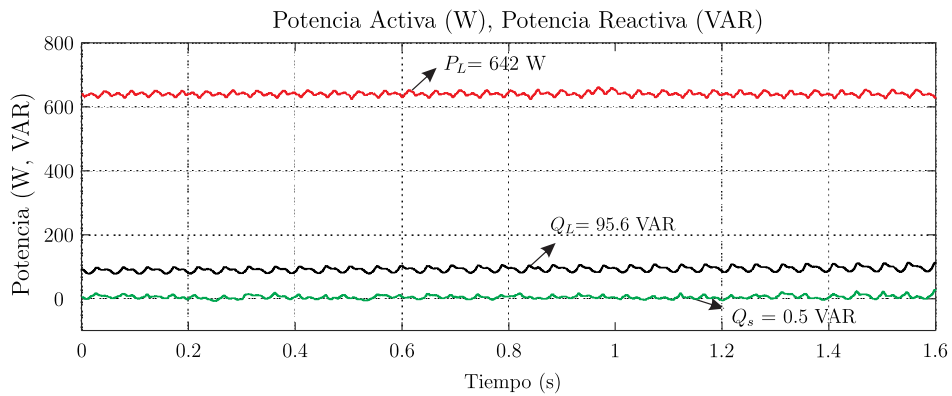


Figura 4.2 Compensación de la potencia reactiva visualizada en el sistema SCADA.

4.3. Compensación de potencia reactiva

En la siguiente sección se presentan los resultados de compensación de la potencia reactiva utilizando un motor de 0.75 Hp como carga reactiva. En la **Figura 4.2** se presentan los resultados de compensación de la potencia reactiva visualizados en el sistema SCADA, en donde $P_L = 642 \text{ W}$ representa la potencia activa de la carga, $Q_L = 98.6 \text{ VAR}$ representa la potencia reactiva de la carga y $Q_s = 0.5 \text{ VAR}$ representa la potencia reactiva de la red eléctrica.

En la **Figura 4.3** se presenta el desfase de voltaje v_s^a y corriente en la red eléctrica i_s^a medidas a través de un osciloscopio del sistema sin compensar, aproximadamente 8 grados y en la **Figura 4.4** se presenta el desfase de voltaje de la red eléctrica v_s^a y corriente en la red eléctrica i_s^a , medidas a través de un osciloscopio una vez realizada la compensación de la potencia reactiva.

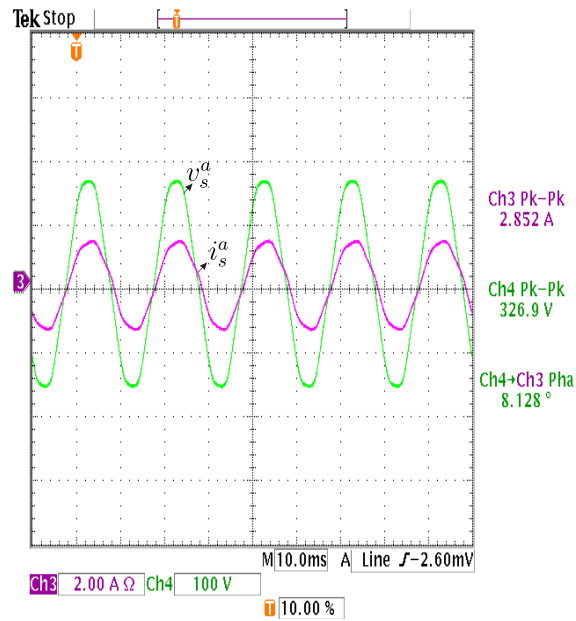


Figura 4.3 Medición de la potencia reactiva no compensada visualizada en el osciloscopio.

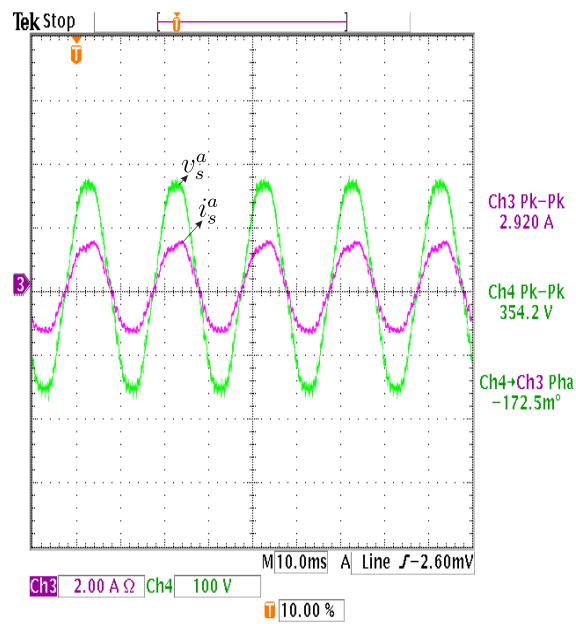


Figura 4.4 Medición de la potencia reactiva compensada visualizada en el osciloscopio.

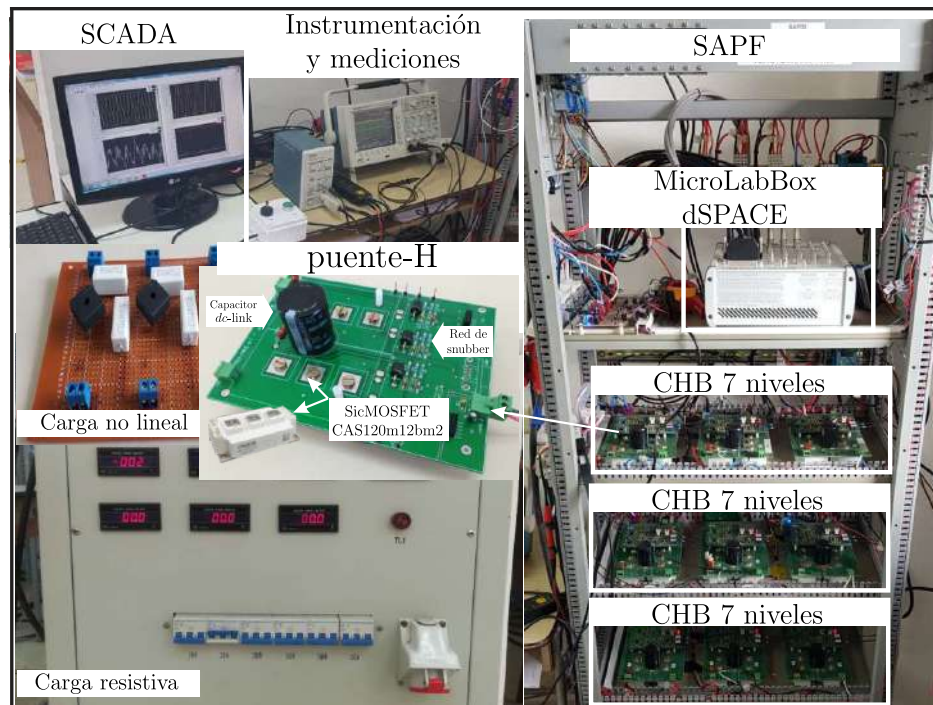
4.4. Compensación de armónicos de corriente

Para la compensación de armónicos de corriente de la red eléctrica, el sistema se conecta a un rectificador trifásico como carga no lineal de tal manera a armónicos de corriente en la red eléctrica. El SAPF utiliza dispositivos de conmutación SiC-MOSFET y un dc -link como se muestra en la **Figura 4.5 (a)**. Luego, para verificar el desempeño de la técnica MPC propuesta, se han realizado varias pruebas experimentales usando los siguientes parámetros: $v_s^\phi = 120$ Vrms, $v_{dc}^* = 85$ V, $C_{dc}^\phi = 23420$ uF, $L_f = 10$ mH, frecuencia portadora $f_c = 1$ kHz para el PSPWM.

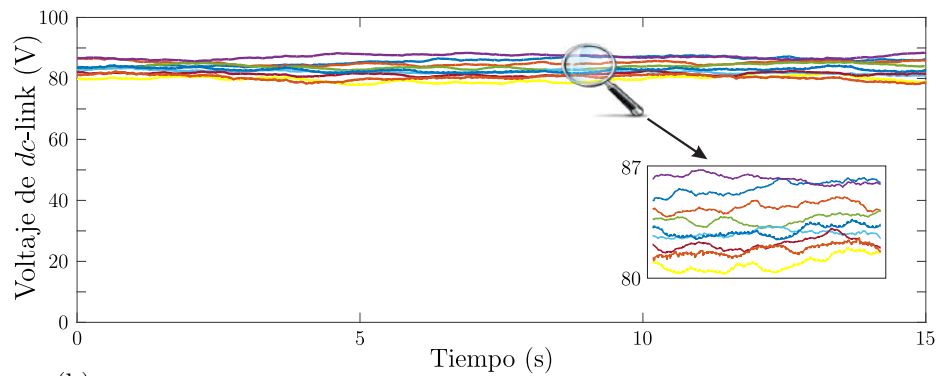
En primer lugar, se analiza la regulación de voltaje del enlace de CC. Los parámetros de control PI son $kp = 0,587$ y $ki = 0,2935$. Entonces, para verificar el control PI que actúa sobre la carga y balance de los voltajes del dc -link, la respuesta dinámica de los voltajes v_{dc}^ϕ se muestra en **Figura 4.5 (b)**. Teniendo en cuenta un voltaje de referencia, se puede observar un balance de los voltajes con un error de ± 5 V lo que representa un error de aproximadamente 5 %.

Luego, se realiza un análisis dinámico del SAPF. **Figura 4.6 (a)** y **Figura 4.6 (b)** muestran la corriente medida i_c^a en la salida del convertidor antes y después de activar el SAPF. Se puede notar, en la **Figura 4.6 (a)**, cómo la corriente de la red i_c^a es compensada con una forma de onda sinusoidal. **Figura 4.6 (b)** incluye el voltaje v_c^a de 7 niveles en la salida del convertidor. En **Figura 4.6 (c)** la respuesta dinámica del voltaje de salida del convertidor v_c^a y la corriente de la red eléctrica i_s^a se presentan cuando ocurre un cambio de carga $R_L = 75 \Omega$ a $R_L = 50 \Omega$. Se puede observar una buena respuesta dinámica con una inyección de corriente baja de alrededor de 2 A pico a pico a 6 A pico a pico. En **Figura 4.6 (d)** se muestra la corriente inyectada por el filtro i_c^a frente a la variación de la carga y la corriente de la red eléctrica i_s^a cuando la carga varía. A continuación, en la **Figura 4.6 (e)** se muestra una prueba del algoritmo de control propuesto frente a una variación del 10 % de los voltajes de la red eléctrica v_s^ϕ y la corriente de carga i_L^a cuando el SAPF está apagado, lo que conduce a una fuente de corriente distorsionada. Sin embargo, cuando se activa el SAPF, bajo el 10 % de variación de los voltajes de la red eléctrica, la corriente de la red eléctrica i_s^a se compensa, como se muestra en la **Figura 4.6 (e)**.

Por último, se ha realizado el análisis de THD de la corriente de la red eléctrica bajo dos condiciones de carga no lineal. **Figura 4.7 (a)** muestra las corrientes de la red eléctrica no compensada (SAPF off) i_s^ϕ . **Figura 4.7 (b)** muestra la i_s^ϕ cuando en SAPF está encendido, donde se puede apreciar la forma de onda sinusoidal. Se ha realizado el mismo análisis $R_L = 75 \Omega$ como se muestra en **Figura 4.7 (d)** y **Figura 4.7 (mi)**. En ambos casos se ha obtenido una reducción considerable de la THD, que corresponde a 29,9 % a 6,4 %, y 27,37 % a 6,8 %, para un $R_L = 100 \Omega$ y $R_L = 75 \Omega$, respectivamente.



(a)



(b)

Figura 4.5 (a) Esquema de bancada experimental del SAPF trifásico basado en CHB de 7 niveles. (b) Mediciones de voltajes de *dc-link*.

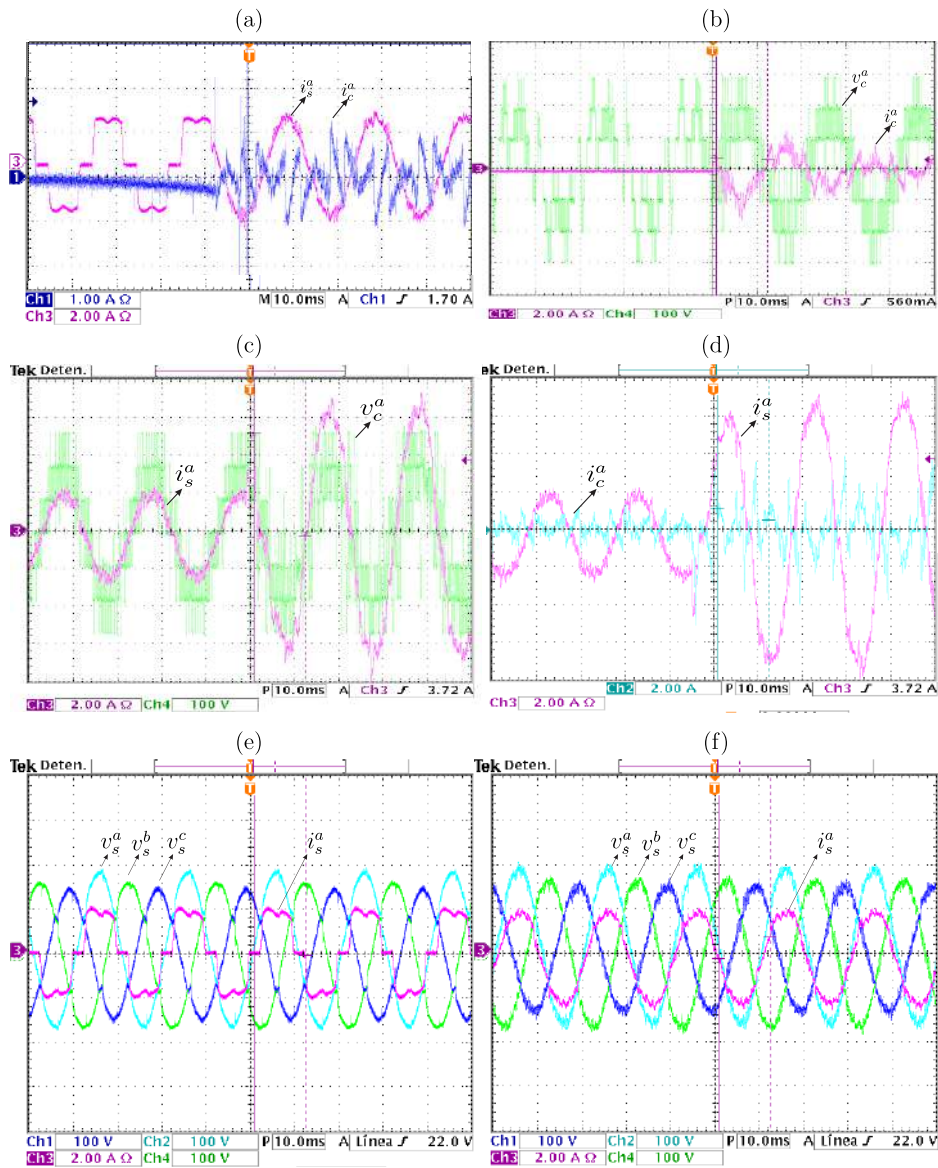
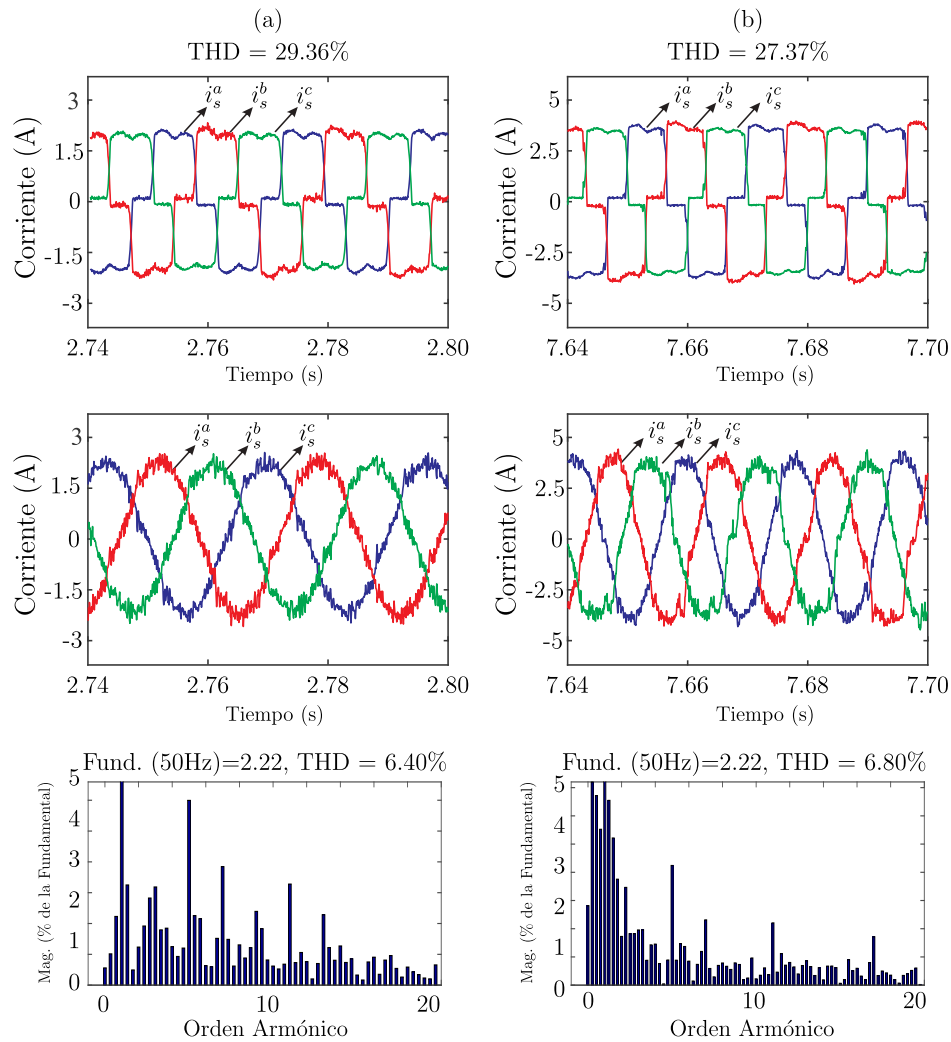


Figura 4.6 Comportamiento transitorio de SAPF, (a) fuente de compensación de armónicos de corriente. (b) voltaje y salida de corriente de SAPF. (c) corriente i_s^a y voltaje v_c^a para cambios instantáneos de resistencia de carga. (d) corriente i_c^a e i_s^c para aumento de carga. (e) Voltajes desequilibrados y corriente de fuente no compensada. (f) corriente de fuente compensada.

**Figura 4.7**

Resultados experimentales de compensación de armónicos de corriente de la red eléctrica considerando una carga no lineal y tres puntos de operación, (a) Corriente de red no compensada para $RL = 100 \, \Omega$, (b) Corriente de red compensada para $RL = 100 \, \Omega$, (c) Nivel de THD de corriente de red compensada para $RL = 100 \, \Omega$. (d) Corriente de red no compensada para $RL = 75 \, \Omega$, (e) Corriente de red compensada para $RL = 75 \, \Omega$, (f) Nivel de THD de corriente de red compensada para $RL = 75 \, \Omega$.

4.5. Conclusiones del capítulo

En el presente capítulo se han presentado los resultados experimentales de la estrategia de control propuesta utilizando el esquema SRF para la generación de la corriente de

referencia aplicado al SAPF trifásico de 7 niveles basado en convertidores en configuración CHB. Se evaluó el SAPF en dos modos de operación, la primera con una carga resistiva-inductiva con el objetivo de compensar la potencia reactiva y la segunda con una carga no lineal con el objetivo de compensar los armónicos de corriente en la red eléctrica. Para la compensación de potencia reactiva se realizaron pruebas para una carga de 95.63 VAR logran disminuir la potencia reactiva de la red eléctrica hasta los 0.5 VAR. Por otro lado, Para la prueba de compensación de armónicos se hicieron pruebas para dos puntos de operación utilizando un rectificador trifásico con una carga resistiva de $100\ \Omega$ y $75\ \Omega$ respectivamente, luego se realizaron mediciones de THD de la corriente de la red eléctrica para esos dos puntos de operación logrando reducir el THD de la red eléctrica de 29.36 % y 27.37 % a 6.40 % y 6.80 % respectivamente.

CAPÍTULO 5

CONCLUSIONES Y TRABAJOS FUTUROS

5.1. Conclusiones

La presente Tesis Doctoral ha abordado el estudio de la estrategia de control predictivo basado en modelo aplicado a un filtro activo trifásico basado en convertidores en configuración puente-H en cascada de 7 niveles, en combinación con la estrategia de modulación SV-PSPWM. Las principales contribuciones y conclusiones se resumen a continuación:

1. Se realizó un estudio teórico de los filtros activos en forma general para luego realizar una taxonomía de las diferentes topologías del convertidor en aplicaciones de SAPF desde el punto de vista de las estrategias de control. Entre las técnicas analizadas resalta el control predictivo debido a sus principales ventajas como su baja complejidad, posibilidad de optimizar múltiples objetivos a la vez con una sola ley de control, la inclusión de restricciones del sistema, la característica discreta de su aplicación en el campo de la electrónica de potencia debido a que el esfuerzo de

control resultante se calcula tomando como referencia un numero de estados finitos de conmutación.

2. Se realizó un análisis teórico mediante herramientas de simulación de la estrategia de control predictivo de corriente en combinación con la modulación SV-PSPWM utilizando dos métodos de generación de referencia las cuales son la IRPT y el SRF. Los resultados teóricos han sido analizados utilizando como figura de merito el MSE y la THD. Los resultados teóricos han demostrado que el control predictivo es una propuesta viable para los dos métodos de generación de referencia mencionados, en términos de seguimiento, compensación de potencia y reducción de los niveles de armónicos de corriente de la red eléctrica. En cuanto a las técnicas de generación de referencia, se ha verificado que el SRF presenta mejores resultados comparativos con respecto a la técnica IRPT, presentando mejores prestaciones en términos de MSE y THD con mejoras cuantificadas en 23.38 % y 22.61 %, respectivamente.
3. Se analizó el uso de la estrategia de control predictivo de corriente en combinación con la modulación SV-PSPWM enfocado a soluciones sub-óptimas para la reducción del espacio de búsqueda del vector óptimo, en el proceso de optimización del control predictivo, en este sentido, se logró la reducción de los vectores de 262144 a 54, lo que implica una reducción de costo computacional haciendo posible la implementación del algoritmo de control propuesto en un dispositivo controlador comercial.
4. Se realizó ensayos experimentales de la estrategia de control predictivo de corriente en combinación con la modulación SV-PSPWM utilizando el método de generación de referencia SRF para la compensación de los armónicos de corriente de la red eléctrica. Los resultados fueron analizados a través de mediciones de la corriente de la carga, la corriente del filtro, corriente de la red eléctrica y voltajes a la salida del convertidor multinivel. Además, agrego un control PI para equilibrar los voltajes de *dc*-link de los capacitores. Se realizaron mediciones con pruebas con cambio de carga y con un desequilibrio en los voltajes de la red eléctrica del 10 %. Los resultados experimentales fueron analizados tomando como figura de merito el MSE y THD, en dos puntos de operación de carga de 100 Ω y 75 Ω respectivamente. La estrategia de control propuesta además de realizar la reducción de los vectores de voltaje en el espacio vectorial de 262144 a 54, ha posibilitado mejorar el perfil de armónico en corriente, reduciendo la THD de la corriente de fase de la red eléctrica de 29.36 %, para la corriente de fase circulante sobre una carga de 100 Ω y 27.37 %, para la corriente de fase circulante sobre una carga de 75 Ω , a 6.40 % y 6.80 %, respectivamente. En este sentido, la mejora en términos de THD para ambas

cargas consideradas en el análisis experimental, puede cuantificarse en 78 % y 75 %, respectivamente.

5.2. Principales aportaciones al estado del arte del control del SAPF

A continuación se presenta el listado de artículos publicados en revistas internacionales arbitradas e indexadas con factor de impacto definido, así como las aportaciones realizadas en conferencias internacionales de relevancia en el área que aborda la Tesis Doctoral.

Producción/Actividad	Número
Aportaciones en revistas internacionales	5
Aportaciones en congresos internacionales	6
Proyectos I+D	1

5.2.1. Aportaciones en revistas internacionales

1. Alfredo Renault, Julio Pacher, Leonardo Comparatore, Magno Ayala, Jorge Rodas y Raúl Gregor, (2022). MPC with Space Vector Phase-Shift PWM (SV-PSPWM) Technique with Harmonic Mitigation Strategy for Shunt Active Power Filters Based on H-Bridge Multilevel Converter. *Frontiers in Energy Research*, 10, 779108.
2. Raul Gregor, Julio Pacher, Alfredo Renault, Leonardo Comparatore and Jorge Rodas, (2022). Model Predictive Control of a Modular 7-Level Converter Based on SiC-MOSFET Devices—An Experimental Assessment. *Energies*, 15(14), 5242.
3. Raul Gregor, Julio Pacher , Alejandro Espinoza, Alfredo Renault , Leonardo Comparatore, (2021). Experimental Validation of the DSTATCOM Based on SiC-MOSFET Multilevel Converter for Reactive Power Compensation. *Journal of Systemics, Cybernetics and Informatics*, 19.
4. Raul Gregor, Julio Pacher , Alejandro Espinoza, Alfredo Renault , Leonardo Comparatore and Magno Ayala, (2021). Harmonics Compensation by Using a Multi-Modular H-Bridge-Based Multilevel Converter. *Energies*, 14, 4698.
5. Julio Pacher, Jorge Rodas, Raul Gregor, Marco Rivera, Alfredo Renault and Leonardo Comparatore, (2018). Efficiency analysis of a modular H-bridge based on SiC MOSFET. *International Journal of Electronics Letters*, 7, 59-67.

5.2.2. Aportaciones en congresos internacionales

1. Renault, A., Ayala, M., Pacher, J., Comparatore, L., Gregor, R., & Toledo, S. (2020). Current control based on space vector modulation applied to three-phase H-Bridge STATCOM. In 2020 IEEE International Conference on Industrial Technology (ICIT) (pp. 1066-1070). IEEE.
2. Toledo, S., Ayala, M., Maqueda, E., Gregor, R., Renault, A., Rivera, M., ... & Wheeler, P. (2020). Active and reactive power control based on predictive voltage control in a six-phase generation system using modular matrix converters. In 2020 IEEE International Conference on Industrial Technology (ICIT) (pp. 1059-1065). IEEE.
3. Renault, A., Ayala, M., Pacher, J., Comparatore, L., Gregor, R., & Rivera, M. (2019). Analysis of H-Bridge STATCOM with Fault Phase Controlled by Modulated Predictive Current Control. In 2019 IEEE CHILEAN Conference on Electrical, Electronics Engineering, Information and Communication Technologies (CHILECON) (pp. 1-5). IEEE.
4. Renault, A., Ayala, M., Comparatore, L., Pacher, J., & Gregor, R. (2018). Comparative study of predictive-fixed switching techniques for a cascaded h-bridge two level statcom. In 2018 53rd International Universities Power Engineering Conference (UPEC) (pp. 1-6). IEEE.
5. Renault, A., Rodas, J., Comparatore, L., Pacher, J., & Gregor, R. (2018). Modulated predictive current control technique for a three-phase four-wire active power filter based on H-bridge two-level converter. In 2018 53rd International Universities Power Engineering Conference (UPEC) (pp. 1-6). IEEE.
6. Comparatore, L., Renault, A., Pacher, J., Rodas, J., & Gregor, R. (2018). Finite control set model predictive control strategies for a three-phase seven-level cascade H-bridge DSTATCOM. In 2018 7th International Conference on Renewable Energy Research and Applications (ICRERA) (pp. 779-784). IEEE.

5.2.3. Proyectos I+D

Participación como investigador asociado en proyecto de investigación financiado por el Conacyt Paraguay, denominado proyecto 14-INV-096, Análisis, diseño e implementación de nuevos sistemas de compensación basados en filtros activos para la mejora de la calidad de la potencia eléctrica.

5.3. Líneas futuras de investigación

Como líneas futuras de investigación derivadas del desarrollo de la Tesis Doctoral se resaltan los siguientes aspectos:

- Se propone la implementación de la etapa de modulación sobre una plataforma FPGA a fin de obtener mayores frecuencias de conmutación mediante el diseño de un modulador de aplicación dedicada dentro del FPGA, de tal manera a reducir el esfuerzo computacional del DSP incluido dentro del controlador dSPACE MicroLabBox. Se espera que el aumento de la frecuencia de conmutación y la reducción del tiempo de muestreo, se traduzca en un mejor rendimiento en términos de MSE y THD en la corriente de salida.
- Se plantea seguir investigando y realizando pruebas experimentales de las estrategias de control enfocadas al balance de los voltajes de los capacitores del *dc*-link, a fin de obtener un mejor balance de los voltajes lo que mejorará la performance de la estrategia de control MPC, ya que se ha podido corroborar mediante ensayos experimentales que la estabilidad del controlador se encuentra vinculada, entre otras cosas, al adecuado balance de los voltajes de *dc*-link.
- Se propone ampliar las estrategias de control a sistemas trifásicos de cuatro hilos, lo que permitiría implementar el SAPF en sistemas con cargas desbalanceadas y con capacidad de eliminación de la corriente del punto neutro, ya que en los sistemas trifásicos las cargas generalmente se encuentran desbalanceadas y esto causa una circulación de corriente por el punto neutro. Esto implicaría la ampliación del hardware del SAPF y la modificación en la generación de referencia.
- Si bien la técnica de control MPC propuesta presenta un buen rendimiento en términos de MSE y la THD, se propone abordar otras estrategias de control no lineales como el control en modo deslizante combinadas con estrategias de modulación SVM, M2PC, PSPWM, LSPWM, etc. Con esto buscaría investigar otras estrategias de control combinadas con modulación, que posibiliten seguir aportando a la mejora de las prestaciones dinámicas del SAPF.

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CAPÍTULO 6

ANEXOS



MPC with Space Vector Phase-Shift PWM (SV-PSPWM) Technique with Harmonic Mitigation Strategy for Shunt Active Power Filters Based on H-Bridge Multilevel Converter

Alfredo Renault*, Julio Pacher, Leonardo Comparatore, Magno Ayala, Jorge Rodas and Raul Gregor

Laboratory of Power and Control Systems (LSPyC), Facultad de Ingeniería, Universidad Nacional de Asunción, Luque, Paraguay

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*Correspondence:

Alfredo Renault
arenault@ing.una.py

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INTRODUCTION

Nowadays, electrical distribution systems present a complex electrical scenario, where different dynamic load devices such as switching power supplies, rectifiers and AC motors are integrated (Habibullin et al., 2014; Mishra et al., 2020). This increasing number of connected devices causes problems such as increased reactive power and the harmonic distortion of the electrical current power grid. Consequently, other issues appear in the distribution grid, for instance, overheating of the conductors, current surges, high current consumption, which leads to resizing connections and possible damage to devices connected to the power grid (Motta and Faundes, 2016; Das et al., 2020). Consequently, various types of equipment have been proposed to solve these power quality problems, namely.

- Shunt Active Power Filters (SAPF), to mitigate current harmonics (Jia et al., 2020).
- Static Distribution Compensators (DSTATCOM), to mitigate reactive power.
- Dynamic Voltage (DVR) to mitigate voltage unbalance disturbances (Ferreira et al., 2017).
- Unified Power Quality Conditioners (UPQC) to compensate for voltage and current quality problems (Irannezhad et al., 2012; Yang et al., 2021).

Within the SAPF literature, it has been studied extensively, from the different topologies of converters such as those based on Voltage Source Inverters (VSI), Neutral Point Clamped (NPC) and Cascade H-Bridge (CHB) converters (Jin et al., 2020; Po-Ngam, 2014). Depending on the configuration, they can consist of two levels or multilevel. CHB multilevel converters are increasingly seen as a promising solution due to their advantages, such as their high conversion

efficiency (Marzo et al., 2021), modular structure (Hekmati et al., 2021), scalability to extend to more levels (Ramos et al., 2020), and higher number of redundant switching states (Comparatore et al., 2017). Note that this system needs a DC-link that can be provided by using a power supply or capacitors. The power supply would increase the costs of the implementation since nine power supplies are required (Wang J. et al., 2020; Wong et al., 2020). For this reason, capacitors with a large capacitance are typically used to emulate a power supply (Qamar et al., 2020). However, the capacitors absorb and deliver energy at the Point of Common Coupling (PCC) point, and between the converters of the same phase, this causes fluctuations in the DC-link voltages and makes variations compared to the reference (Bosch et al., 2017; Tareen and Mekhilef, 2017).

From the control's point of view, the Proportional-Integral-Derivative (PID) and the Hysteresis control are the most applied techniques for power electronic converters. However, non-linear techniques such as the sliding mode control and the Model-based Predictive Control (MPC) have attracted attention in recent years. MPC has some advantages over the conventional linear current controller, such as important flexibility, including constraints and a suitable dynamic response (Rodas et al., 2021). However, MPC has one of its main disadvantages its high computational burden that makes it difficult to implement in complex systems. Also, MPC has a variable switching frequency that causes more significant stress on the switching devices and introduces non-linearities that propagate in the injected current. To solve MPC's variable switching behaviour, some modulation techniques such as Pulse-Width Modulator (PWM), Space Vector Modulation (SVM) (Li and Zhao, 2020; Ronanki and Williamson, 2018), and Modulated MPC have been included in the control scheme. Though, most of them are applied to two-level SAPF. On the other hand, for multilevel SAPF based on CHB, the most usual modulator are Phase-Shift PWM (PSPWM) and Level-Shift PWM (LSPWM). PSPWM has some advantages such as easy compression and that it performs a natural balancing of the capacitor voltages (Rao et al., 2020; Ferreira et al., 2017).

In what follows, some recent works carried out regarding the control and modulation techniques used in this work are presented. In (Tarisciotti et al., 2016), an MPC for a SAPF with the fixed switching frequency is proposed and named M2PC. The modulation is included in the MPC structure and then applied to the SAPF based on a two-level VSI to reduce THD currents. A fast multilevel SVPWM method based on the imaginary coordinate with direct control of redundant vectors or zero sequence components is proposed in (Yuan et al., 2020). This latter presents a modification of the SVPWM technique based on the imaginary coordinate system, which is applied to different topologies of multilevel converters. In (Li et al., 2021), a sliding mode SVPWM method for an HTS SAPF is studied. This non-linear controller is combined with the SVPWM technique to be applied to the two-level SAPF. A simplified 3-D NLM-Based SVPWM technique with voltage-balancing capability for three-level NPC cascaded multilevel converter is proposed in (Lin et al., 2019) that presents a modification of the SVPWM modulation technique based on the closest level modulation, applied to the multilevel NPC converter.

The previous works show different applications of both the control and the modulation technique, where the proposal of this article is the MPC control technique in combination with the SVPWM modulation technique applied to a SAPF based on cascaded H-bridge converters of 7 levels. Then, in this paper, a method of reducing the switching states using the space voltage vectors consists of obtaining the switching states for the three-level configuration. Once the vectors are selected, they are projected for the 7 levels' configuration or more. The main advantage of this technique is the reduction of the computational burden by reducing the voltage vectors that allow the possibility of real-time implementation.

The main contribution of this research is the combination of the MPC with the SV-PSPWM technique applied to the 7-level CHB converter. In addition, a PI control is implemented to balance the DC-link voltages in the experimental platform. The proposed control scheme optimizes the prediction with voltage estimates in combination with the input and output signs of each CHB per phase, avoiding using a constant reference. The proposed MPC controller has been implemented in dSPACE-MicroLabBox platform. Also, tests of the control scheme have been carried out on the experimental bench using different operating points.

The article is organized as follows. In the following section, the mathematical model of SAPF applied in a three-phase system based on 7-level CHB SAPF topology is first presented. Subsequently, the current reference generator, the DC-link control, the predictive model, and the PSPWM modulation are presented. In **Section 3** the experimental results are shown and finally in **Section 4** the conclusions of the work are presented.

FUNDAMENTAL CONCEPTS, ISSUES, AND PROBLEMS

Three-phase SAPF Based on Multimodular CHB Converter Model

The right side of **Figure 1A** shows the general connection scheme of the multimodular SAPF based on 7-level CHB converters to a three-phase distribution power grid at the PCC point. Each CHB module is made up of a DC-link C_{dcx}^{ϕ} with a voltage v_{dcx}^{ϕ} and four SiC-MOSFET switching devices, connected 3 CHBs in series per phase. Each CHB cell consists of four trigger signals $S_{xy}^{\phi} \in [0, 1]$, where S represents the trigger signals, $x = [1, 2, 3]$ the number of CHB corresponding per phase, $y = S_{11}, S_{12}, S_{31}$ and S_{32} represents the matrix of switching states according to Table 1, shown in **Figure 1C**, for phase a , performing the same analysis for the other phases and finally $\phi = [a, b, c]$ corresponds to the phases of the three-phase electrical power grid.

The mathematical model of the SAPF based on 7-level CHB converters is obtained by applying Kirchhoff's laws from the DC-link in the outgoing direction of the converter to the AC side of the electrical grid. The dynamics of the system is obtained:

$$\frac{di_c^{\phi}(t)}{dt} = \frac{v_s^{\phi}(t)}{L_f} - \frac{v_c^{\phi}(t)}{L_f} - \frac{R_f i_c^{\phi}(t)}{L_f} \quad (1)$$

where i_c^{ϕ} represents the current injected by the filter at the PCC point in each phase, v_s^{ϕ} the voltages of the electrical power grid, L_f

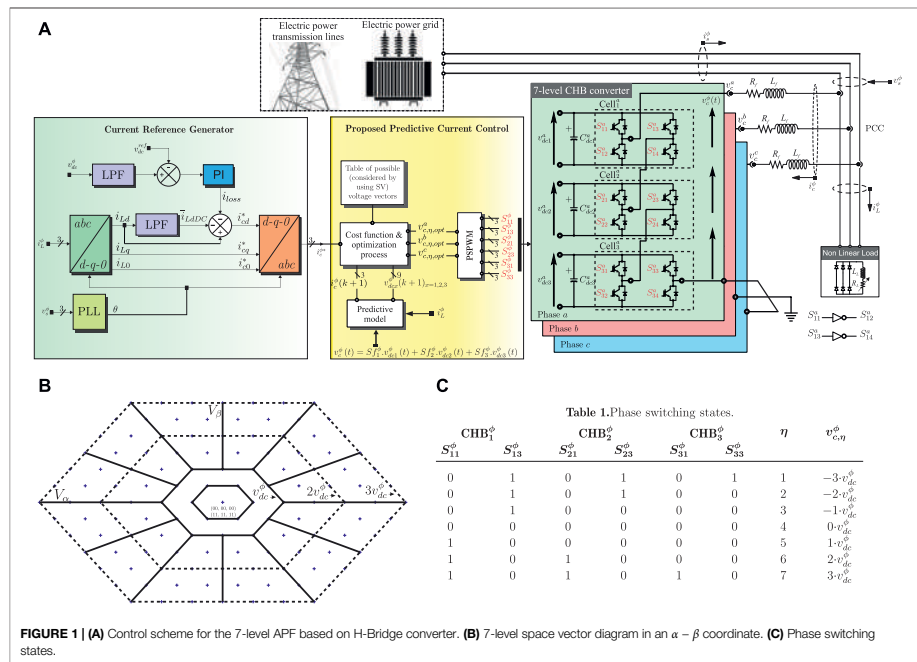


FIGURE 1 | (A) Control scheme for the 7-level APF based on H-Bridge converter. **(B)** 7-level space vector diagram in an $\alpha-\beta$ coordinate. **(C)** Phase switching states.

the output inductance of the filter, v_c^ϕ the output voltage of the converter and R_f the parasitic resistance of the inductance. Due to the CHB topology that uses independent DC-link using capacitors in combination with the activation signals, the model of the converter voltages is obtained:

$$v_c^\phi(t) = (S_{f11}^\phi - S_{f12}^\phi) v_{dc1}^\phi(t) + (S_{f21}^\phi - S_{f22}^\phi) v_{dc2}^\phi(t) + (S_{f31}^\phi - S_{f32}^\phi) v_{dc3}^\phi(t) \quad (2)$$

From this, the control model is obtained, avoiding using a fixed reference voltage. Instead, the measured voltages of each converter with its corresponding sign are used to get the real voltage outputs of the converter.

Current Reference Generation

The calculation of the reference currents i_c^{ref} is based on the Synchronous Reference Frame (SRF). Figure 1A (left part) shows the detail procedure. First, the angle θ of the electrical power grid is obtained through a Phase Locked Loop (PLL). This angle is used to transform from $a-b-c$ plane to the $d-q-0$ plane, and viceversa. Then, a Low-Pass Filter (LPF) is used to eliminate the AC component of the load measurement current I_{Ld} (d-component).

Before the operation of the SAPF, all capacitors need to be charged to the reference voltage v_{dc}^{ref} . The SAPF during its operation can absorb or inject current into the electrical grid. This latter produces the charge and discharge of the C_{dcx} capacitors of each CHB. Consequently, it causes the unbalance of the DC-link voltages (Li et al., 2017). To solve this issue, a Proportional-Integral (PI) controller is used that provides the loss current i_{loss} of the capacitors which is absorbed from the electrical grid (Sohagh et al., 2020). Therefore, the loss current represents the consumption currents in each phase of the C_{dcx} capacitors, and the PI control is using to compensate this loss in such a way as to balance the voltage of the DC-link v_{dc}^ϕ (Ray et al., 2017). The equations corresponding to the PI control in discrete time are shown below (Pandurangan et al., 2020; Zhou et al., 2020):

$$e^\phi(k) = v_{dc}^{ref} - v_{dc1}^\phi \quad (3)$$

$$i_{loss}^\phi = i_{loss}^\phi(k-1) + kp(e^\phi(k) - e^\phi(k-1)) + T_{PI} ki e^\phi(k) \quad (4)$$

$$i_{loss}^\phi = \frac{1}{3} \sum_{\phi=a,b,c} i_{loss}^\phi \quad (5)$$

where $e^\phi(k)$ represents the error between the reference and the previously filtered measured voltages v_{dc1}^ϕ . Then, the loss current i_{loss}^ϕ is calculated, $i_{loss}^\phi(k-1)$ being the loss current estimated in

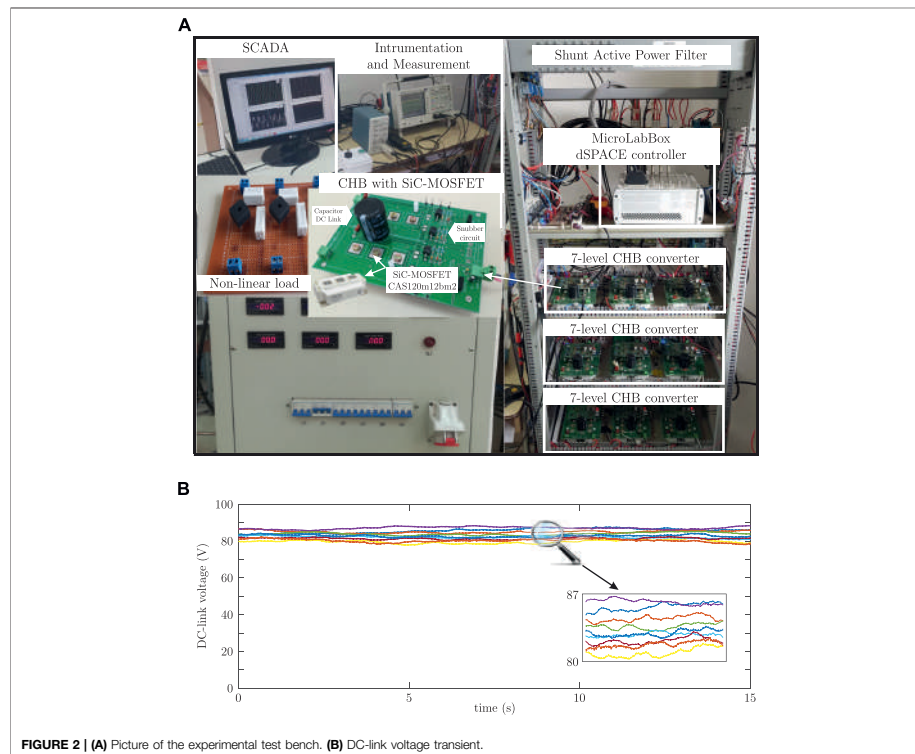


FIGURE 2 | (A) Picture of the experimental test bench. **(B)** DC-link voltage transient.

the previous instant, $e(k-1)$ the voltage error calculated during the last instant, T_{PI} represents the PI controller actuation time and finally i_{loss} which represents the average of the loss currents of each phase. Then, since the reference in d component of the current reference is obtained, the inverse Park transformation is applied to find the reference currents i_c^{*ab} to be used by the proposed model predictive current controller.

Predictive Model

The predictive model can be obtained from Eq. 1 by using a forward-Euler discretization method (Boukezata et al., 2017). Euler's method is the most basic explicit method for numerical integration of ordinary differential equations and consequently carries a low computational burden, which benefits the experimental implementation (Jia et al., 2020). The SAPF discrete-time model is given by:

$$i_c^\phi(k+1) = \left(1 - \frac{R_f T_s}{L_f}\right) i_c^\phi(k) + \frac{T_s}{L_f} (v_c^\phi(k) - v_s^\phi(k)) \quad (6)$$

where k identifies the actual discrete-time sample, T_s is the sampling time, and $i_c^\phi(k+1)$ is a prediction of the SAPF phase currents made at sample k . Also, in Eq. 6, $i_c^\phi(k)$ corresponds to the measured current at the output filter in the current sampling time k . While $v_s^\phi(k)$ corresponds to the measured phase voltage in the electrical grid at the same sampling time k . Then, these measured values are used by the predictive. Last, $v_c^\phi(k)$ is computed at each sampling instant using the discrete-time version of Eq. 2, and uses the measured DC-link capacitor voltages $v_{dc1}^\phi(k)$.

Cost Function and Optimization Process

In MPC technique, a cost function is calculated for different switching state conditions of a system under study to find the most suitable voltage vector. In other words, for all feasible switching state conditions, the cost function is computed, and then, the one that minimizes a pre-defined cost function is selected and applied during the next sampling time to the system. In this paper, the cost function is defined as the error between the prediction and the reference. In the three-phase

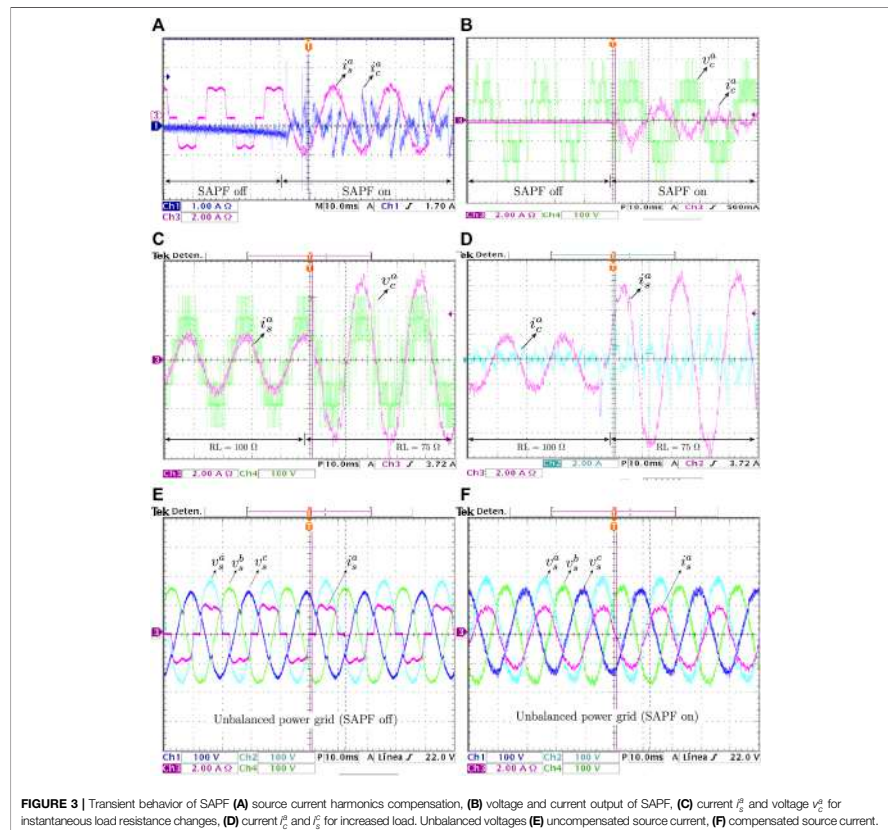


FIGURE 3 | Transient behavior of SAPF (A) source current harmonics compensation, (B) voltage and current output of SAPF, (C) current i_s^a and voltage v_s^a for instantaneous load resistance changes, (D) current i_s^a and i_s^b for increased load. Unbalanced voltages (E) uncompensated source current, (F) compensated source current.

control scheme, the cost functions are evaluated independently from the following equations:

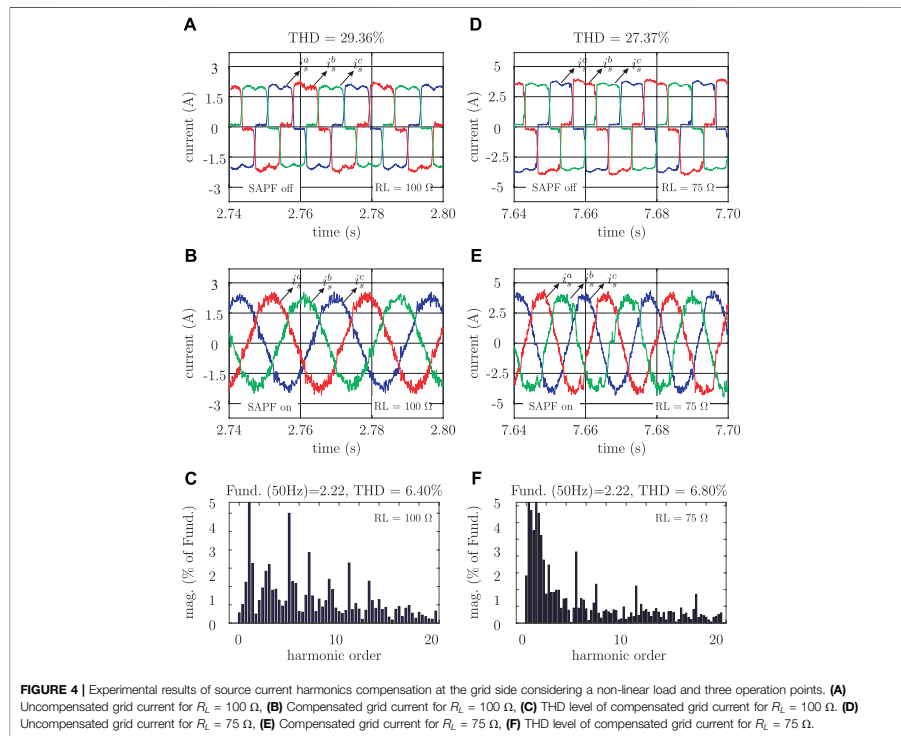
$$\begin{aligned} g^a &= \|i_c^{a*} - i_c^a(k+1)\|^2 \\ g^b &= \|i_c^{b*} - i_c^b(k+1)\|^2 \\ g^c &= \|i_c^{c*} - i_c^c(k+1)\|^2. \end{aligned} \quad (7)$$

Next, the optimization algorithm selects the optimal vector $S_{\eta,opt}^a$ which corresponds to the voltage that minimizes the cost function, to then be sent to the modulator stage.

Space Vector Phase-Shift PWM Technique

As mentioned in the previous section, the optimization algorithm evaluates all feasible switching states. SAPF based on 7-level CHB

converters, consists of $2^{\psi\%}$ which is equivalent to 262 144 voltage vectors, where $S_{\psi} = 6$ corresponds to the six control signals and $\psi = 3$ represents the three CHBs per phase. This latter leads to a high computational burden that makes it impossible to be implemented in digital signal processors available today. Therefore, in this paper, a modulation structure that consists of a combination of the vector space with phase shift modulation is proposed. The aim of this approach is to reduce the computational cost by reducing the number of vectors using as a base of 3-level CHB topology corresponding to one CHB per phase, where the vectors are represented as the first and second hexagons delineated as shown in Figure 1B, the third and fourth hexagon represent the second level by adding a CHB, the fifth and sixth hexagon define the third level by adding a third CHB (He et al., 2020). To



reduce the number of vectors, the first-level vectors extrapolate to the second and third levels. For instance, if the optimal switching states correspond to the first level are (1 0 1) to select the optimal voltage vectors corresponding to the second level is (2 0 2), the same analysis is carried out for the voltage vectors corresponding to the third level. This proposal significantly reduces the interactions from 264 144 to 54 corresponding to the number of points in the diagram in vector space and thus reducing the computational cost and making possible the real-time implementation (Wang C. et al., 2020; Yuan et al., 2020).

Once the optimal voltage level has been selected, the PSPWM is carried out, which consists of three triangular carriers $\frac{180^\circ}{3}$ out of phase with each other with the same amplitude and the same frequency to obtain the activation times of the trigger signals (Gregor et al., 2021).

$$v_{ct}^\phi = \frac{v_{c, \eta, opt}^\phi}{3} \quad (8)$$

where v_{ct}^ϕ is a normalized modulator between -1 and 1 , and $v_{c, \eta, opt}^\phi$ are the optimal voltage levels selected in the vector space. To make the thing clearer, Algorithm 1 summarizes the optimization process.

Algorithm 1. Optimization algorithm of the proposed modulated MPC current controller.

1. Initialize $g_{opt}^\phi := \infty$, $g_{opt}^\phi := \infty$, $g_{opt}^\phi := \infty$, $\eta := 0$
2. Compute the current references
3. **while** $\eta \leq \varepsilon$ **do**
4. $S_{\eta}^\phi \leftarrow S_{\eta}^\phi \forall \eta \in 1, 2, 3$
5. Calculate the prediction currents
6. Compute the cost function
7. **if** $g^\phi < g_{opt}^\phi$ **then**
8. $g_{opt}^\phi \leftarrow g^\phi$, $S_{opt}^\phi \leftarrow S_{\eta}^\phi$
9. **end if**
10. **if** $g^\phi < g_{opt}^\phi$ **then**
11. $g_{opt}^\phi \leftarrow g^\phi$, $S_{opt}^\phi \leftarrow S_{\eta}^\phi$
12. **end if**
13. **if** $g^\phi < g_{opt}^\phi$ **then**
14. $g_{opt}^\phi \leftarrow g^\phi$, $S_{opt}^\phi \leftarrow S_{\eta}^\phi$
15. **end if**
16. $\eta := \eta + 1$
17. **end while**
18. Compute the modulation signals
19. Get the turn-on times of the firing signals
20. Apply the firing signals.

EXPERIMENTAL ASSESSMENT

The DSPACE MicroLabBOX was used as controller in an experimental bench of SAPF based on 7-level CHB connected to a balanced power grid with a non-linear load. Each converter uses a SiC-MOSFET switching devices and a DC-link as shown in **Figure 2**. Then, to verify the performance of the proposed MPC technique, several experimental tests have been carried out using the following parameters: $v_s^\phi = 120$ Vrms, $v_{dc}^{ref} = 85$ V, $C_{dc} = 23\,420$ uF, $L_f = 10$ mH, carrier frequency $f_c = 1$ kHz for the PSPWM.

First, the DC-link voltage regulation is analyzed. The PI control parameters are $kp = 0.587$ and $ki = 0.293$ 5. So, to verify the PI control that acts on the load and balance of the DC-link voltages, the dynamic response of the voltages v_{dc}^ϕ is shown in **Figure 2B**. Taking into account a reference voltage $v_{dc}^{ref} = 85$ V, a balance of the voltages can be observed with an error of ± 5 V which represents an error of approximately 5%.

Then, a dynamic analysis of the SAPF is performed. **Figures 3A,B** show the measured current i_a^u at the converter output before and after activating the SAPF. It can be notice, in **Figure 3A**, how the grid current i_c^u is compensated with a sinusoidal waveform. **Figure 3B** includes the voltage v_c^u of 7 levels at the converter output. In **Figure 3C** the dynamic response of the converter output voltage v_c^u and the electrical power grid current i_s^u are presented when a load change occurs $R_L = 75\ \Omega$ to $R_L = 50\ \Omega$. A good dynamic response can be observed with a low current injection of about 2 A peak-to-peak to 6 A peak-to-peak. In **Figure 3D** the current injected by the filter i_c^u is shown against the variation of the load and the current of the electrical power grid i_s^u when the load varies. Next, in **Figure 3E** a test of the proposed control algorithm is shown against a variation of 10% of the voltages of the electrical power grid v_s^ϕ and the load current i_L^ϕ when the SAPF is off, which leads to an distorted source current. However, when the SAPF is activated, under the 10% of variation of the voltages of the electrical grid, the current of the electrical power grid i_s^u compensated, as show in **Figure 3E**.

Last, the analysis of the Total Harmonic Distortion (THD) of the electrical grid current under two non-linear load conditions has been carried out. **Figure 4A** shows the uncompensated (SAPF off) electrical power grid currents i_s^ϕ . **Figure 4B** shows the i_s^ϕ when en SAPF is on, where it can be appreciated the sinusoidal waveform. The same analysis has been performed $R_L = 75\ \Omega$ as depicted in

Figure 4D,E. In both cases, a considerable reduction of the THD has been obtained, that corresponds to 29.9–6.4%, and 27.37 to 6.8%, for a $R_L = 100\ \Omega$ and $R_L = 75\ \Omega$, respectively.

CONCLUSION

This paper presented the real-time implementation of a model predictive current controller equipped with a modulation stage of a SAPF based on 7-level CHB converters, using SiC-MOSFET switching devices. The novel control scheme combines the concepts of model predictive control with the SV-PSPWM technique with the aim to reduce the computational burden. In addition, PI control is added to balance the DC-link voltages of the capacitors. The proposed control scheme has been validated experimentally. It has been shown that the proposed control can reduce 80% of THD caused by non-linear loads. Moreover, the robustness and effectiveness have been demonstrated under different operating points in both, in steady and transient conditions. Future works may include a comparative study of the proposed control schemes against classic control methods.

DATA AVAILABILITY STATEMENT

The original contributions presented in the study are included in the article/Supplementary Material, further inquiries can be directed to the corresponding author.

AUTHOR CONTRIBUTIONS

AR conceived the idea for this paper. AR, JP and JR were responsible for the primary writing of the manuscript, while LC, MA and RG were responsible for revising the manuscript. All authors contributed to the article and approved the submitted version.

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Article

Model Predictive Control of a Modular 7-Level Converter Based on SiC-MOSFET Devices—An Experimental Assessment [†]

Raúl Gregor , Julio Pachter , Alfredo Renault , Leonardo Comparatore  and Jorge Rodas  *

Laboratory of Power and Control Systems (LSPyC), Facultad de Ingeniería, Universidad Nacional de Asunción, Luque 2060, Paraguay; rgregor@ing.una.py (R.G.); jpachter@ing.una.py (J.P.); arenault@ing.una.py (A.R.); lcomparatore@ing.una.py (L.C.)

* Correspondence: jrodas@ing.una.py

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Abstract: Power converter technology has expanded into a wide range of low, medium, and high power applications due to the ability to manage electrical energy efficiently. In this regard, the modular multilevel converter has become a viable alternative to ensure an optimal harmonic profile with a sinusoidal voltage at the load side. Model predictive control (MPC) is a state-of-the-art technique that has been successfully used to control power electronic converters due to its ability to handle multiple control objectives. Nevertheless, in the classical MPC approach, the optimal vector is applied during the whole sampling period producing an output voltage. This solution causes an unbalanced switching frequency of the power semiconductor, which then causes unbalanced stress on the power devices. Modulation strategies have been combined with MPC to overcome these shortcomings. This paper introduces the experimental assessment of a 7-level converter combining a simple phase shift multicarrier pulse-width modulation approach with the MPC technique. A custom test-bed based on SiC-MOSFETs switches is used to validate the proposal.

Keywords: model predictive control; phase shift multicarrier pulse-width modulation; modular converter; multilevel converter



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1. Introduction

Power converter technologies play an increasingly important role in many applications mainly due to their ability to efficiently manage electrical energy [1]. In this regard, the high penetration of power electronic converters has been justified primarily because of the growth of the electricity generated by renewable energies such as solar and wind [2]. Since all power converters connected to the grid must fulfill the grid codes, power quality has recently become one of the main issues to solve [3,4]. A power quality problem can be seen as the divergence of magnitude and frequency from the ideal sinusoidal waveform [5,6]. This divergence typically impacts currents and voltage at the grid side; the load side has been proposed in several papers to address the power quality issues at the load side [7,8]. The dizzying advance of power converters has been enhanced by developing high-performance microprocessors capable of implementing complex nonlinear digital controllers. The field of power electronic semiconductors has recently developed new high-speed switching devices with tremendous low on-state loss. One of the most promising power electronic semiconductors is the SiC-MOSFET used in this paper. As a result, new power electronic converters can be smaller than the classical ones [9].

Conventional two-level voltage source converters (2L-VSCs) are still one of the most used converters for many applications, and, as all VSCs, they are considered the fundamental component in the conversion energy system. However, the reduced number of levels of 2L-VSCs cause loss problems and poor power quality due to their bad harmonic profile [10,11]. To solve this issue, the modular multilevel converter (MMC) has drawn the

attention of both industry and academic sectors due to its capability to generate sinusoidal voltages and currents with a low content of harmonic distortions at the load side. Among these MMC topologies, the cascade H-Bridge (CHB) is a popular choice because of its modularity, which simplifies the extension for a higher number of levels of the MMC. Moreover, the MMC does not demand a vast number of flying capacitors or clamping diodes [12]. Consequently, the CHB-based MMC is currently a competitive choice in the new era of VSCs [13].

Commonly the CHB-based MMC uses IGBT as switching. Nevertheless, the SiC-MOSFET has been used as an alternative mainly because it can reach higher switching frequencies than IGBT devices [14,15]. Yet, it is not enough to incorporate faster switching to the MMC to improve the power quality [16,17]. Instead, it is essential to manage this problem with a suitable controller. In this regard, model predictive control (MPC) has been successfully used to control VSCs due to its ability to handle multiple control goals and constraints, straightforward implementation, and quick transient response [18,19]. However, the MPC scheme operates with variable frequency leading to a spread switching spectrum [20]. To eliminate the variable switching frequency behavior of the classical MPC, this article introduces a fixed switching frequency MPC (FSF-MPC) based on a phase shift multicarrier pulse-width modulation (PSM-PWM) approach [21,22] and the experimental assessment of the CHB-based MMC [23].

This article is divided as follows. Section 2 introduces the mathematical model of the CHB-based MMC topology. Then, in Section 3, the MMC's predictive model is derived, and the proposed MPC strategy is presented. In Section 4, some figures of merits are used as a reference to analyze the obtained experimental results. Finally, the main conclusions of this work are given in the last section.

2. Proposed 7-Level MMC Topology

Figure 1 shows the proposed MMC scheme. Each MMC has four SiC-MOSFETs and is fed by an independent dc-link. To obtain the 7-level MMC, connecting in a series of three cells is necessary for each phase. S_{xy}^ϕ represent the firing signals, with being ϕ the phase a , b , or c , while x is the cell number in each phase and y the switching device in each cell ($y = 1, 2, 3$, or 4). Some firing signal combinations are shown in Table 1 for phase “a”. The firing signals for phases b and c can be obtained likewise, taking into account the permitted combinations and avoiding short circuits [24,25].

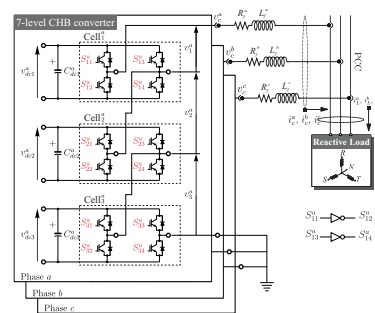


Figure 1. Modular multilevel converter based on cascade H-Bridge.

Table 1. Possible combinations of firing signals.

S_{η}^a							η	$v_{c,\eta}^a$
S_{11}^a	Cell ₁ ^a S_{13}^a	S_{21}^a	Cell ₂ ^a S_{23}^a	S_{31}^a	Cell ₃ ^a S_{33}^a			
0	0	0	0	0	0	0	1	$0 \cdot v_{dc}^a$
0	0	0	0	0	0	1	2	$-1 \cdot v_{dc}^a$
0	0	0	0	1	0	0	3	$1 \cdot v_{dc}^a$
.	.	.	.	.	.	.	.	.
0	1	0	1	0	0	0	21	$-2 \cdot v_{dc}^a$
0	1	0	1	0	1	1	22	$-3 \cdot v_{dc}^a$
.	.	.	.	.	.	.	.	.
1	0	1	0	1	0	0	43	$3 \cdot v_{dc}^a$
.	.	.	.	.	.	.	.	.
1	0	1	0	1	1	1	44	$2 \cdot v_{dc}^a$
.	.	.	.	.	.	.	.	.

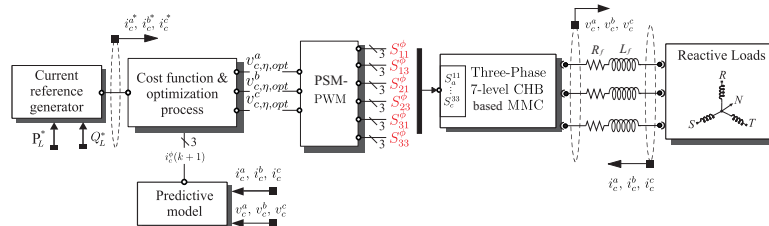
Figure 2 depicts the proposed FSF-MPC control that uses the explicit MMC's mathematical model to compute the predictive behavior of the control actions for every switching state. It is essential to highlight that the 7-level CHB-based MMC is tied to the load through an RL filter. Kirchhoff's circuit laws can be used to obtain the system's dynamic. The following equation is the state-space representation obtained using Kirchhoff's rules on the AC side.

$$\begin{bmatrix} \dot{i}_c^a(t) \\ \dot{i}_c^b(t) \\ \dot{i}_c^c(t) \end{bmatrix} = \mathbb{F} \begin{bmatrix} i_c^a(t) \\ i_c^b(t) \\ i_c^c(t) \end{bmatrix} + \mathbb{G} \begin{bmatrix} -v_c^a(t) \\ -v_c^b(t) \\ -v_c^c(t) \end{bmatrix}, \quad (1)$$

where

$$\mathbb{F} = \begin{bmatrix} -\frac{R_f}{L_f} & 0 & 0 \\ 0 & -\frac{R_f}{L_f} & 0 \\ 0 & 0 & -\frac{R_f}{L_f} \end{bmatrix}, \quad \mathbb{G} = \begin{bmatrix} \frac{1}{L_f} & 0 & 0 \\ 0 & \frac{1}{L_f} & 0 \\ 0 & 0 & \frac{1}{L_f} \end{bmatrix}. \quad (2)$$

L_f represents the inductive filter, which has a parasitic resistance (R_f) that is connected between the point of common coupling (PCC) and the MMC's output.

**Figure 2.** Proposed FSF-MPC control scheme applied to the 7-level MMC.

3. MMC Predictive Model

A forward-Euler discretization procedure has been used to reduce the computational burden of the FSF-MPC. Then, the predictive model can be obtained from (1), with the following equation as the MMC discrete-time model [26,27].

$$\begin{bmatrix} \hat{i}_c^a(k+1) \\ \hat{i}_c^b(k+1) \\ \hat{i}_c^c(k+1) \end{bmatrix} = \mathbb{A} \begin{bmatrix} i_c^a(k) \\ i_c^b(k) \\ i_c^c(k) \end{bmatrix} + \mathbb{B} \begin{bmatrix} -v_c^a(k) \\ -v_c^b(k) \\ -v_c^c(k) \end{bmatrix}, \quad (3)$$

where

$$\mathbb{A} = \begin{bmatrix} a_1 & 0 & 0 \\ 0 & a_1 & 0 \\ 0 & 0 & a_1 \end{bmatrix}, \mathbb{B} = \begin{bmatrix} \frac{T_s}{L_f} & 0 & 0 \\ 0 & \frac{T_s}{L_f} & 0 \\ 0 & 0 & \frac{T_s}{L_f} \end{bmatrix}, \quad (4)$$

with $a_1 = \left(1 - \frac{R_f T_s}{L_f}\right)$ and T_s as the sampling time.

3.1. Current Reference Generation

The FSF-MPC technique requires the previous calculation of the reference currents to calculate the cost function in (8). Therefore, firstly, we must select the active and reactive power reference P_L^* and Q_L^* to be applied to the load side, considering that the voltage references v_{sc}^ϕ are the maximum voltages of the fundamental frequency at the output of the multilevel converter. Using the Clarke transformation matrix ($\mathbf{T}$), the currents and voltages can be represented in static reference frame $\alpha - \beta$ as:

$$\begin{bmatrix} v_{sc}^\alpha \\ v_{sc}^\beta \end{bmatrix} = \underbrace{\sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}}_{\mathbf{T}} \begin{bmatrix} v_{sc}^a \\ v_{sc}^b \\ v_{sc}^c \end{bmatrix}. \quad (5)$$

Then, the relationship between the active and reactive power, as a function of the current references in $\alpha - \beta$ subspace can be represented by:

$$\begin{bmatrix} i_c^{\alpha*} \\ i_c^{\beta*} \end{bmatrix} = \frac{1}{(v_{sc}^\alpha)^2 + (v_{sc}^\beta)^2} \begin{bmatrix} v_{sc}^\alpha & v_{sc}^\beta \\ v_{sc}^\beta & -v_{sc}^\alpha \end{bmatrix} \begin{bmatrix} P_L^* \\ Q_L^* \end{bmatrix}. \quad (6)$$

The phase current references used in the optimization process are:

$$\begin{bmatrix} i_c^{a*} \\ i_c^{b*} \\ i_c^{c*} \end{bmatrix} = \underbrace{\sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}}_{\mathbf{T}^{-1}} \begin{bmatrix} i_c^{\alpha*} \\ i_c^{\beta*} \\ 0 \end{bmatrix}. \quad (7)$$

3.2. Cost Function and Optimization Process

The proposed fixed switching frequency controller is based on the MPC approach and makes explicit use of an optimization process to minimize a definite cost function, represented by (8). The cost function evaluates the current tracking error in each sampling period using the prediction model and considers all possible firing signal combinations.

$$\begin{aligned} g^a &= \| i_c^{a*} - \hat{i}_c^a(k+1) \|^2, \\ g^b &= \| i_c^{b*} - \hat{i}_c^b(k+1) \|^2, \\ g^c &= \| i_c^{c*} - \hat{i}_c^c(k+1) \|^2. \end{aligned} \quad (8)$$

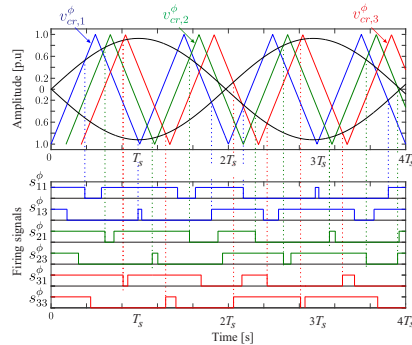
Considering $n_c = 3$ cells per phase connected in cascade, we need $2n_c = 6$ firing signals to control the output voltages (v_c^ϕ). This produces sixty-four ($\epsilon = 2^{2n_c} = 64$) firing signals to be evaluated in the optimization process. After evaluating the cost function for all possible combinations of firing signals, the optimization algorithm selects the optimum vector $S_{\eta,opt}^\phi$ for each firing signal of each cell and applies the optimal vector during a sampling period. The optimization process can be summarized in the pseudocode represented in Algorithm 1.

Algorithm 1 Pseudocode of the optimization process applied to the FSF-MPC current controller

```

1. Initialize  $g_{opt}^a := \infty, g_{opt}^b := \infty, g_{opt}^c := \infty, \eta := 0$ 
2. Compute the current references (7).
3. while  $\eta \leq \epsilon$  do
4.    $S_{\eta}^{\phi} \leftarrow S_{xy}^{\phi} \forall x \& y = 1, 2, 3$ 
5.   Calculate the prediction currents (3).
6.   Compute the cost function, (8).
7.   if  $g^a < g_{opt}^a$  then
8.      $g_{opt}^a \leftarrow g^a, S_{opt}^a \leftarrow S_{\eta}^a$ 
9.   end if
10.  if  $g^b < g_{opt}^b$  then
11.     $g_{opt}^b \leftarrow g^b, S_{opt}^b \leftarrow S_{\eta}^b$ 
12.  end if
13.  if  $g^c < g_{opt}^c$  then
14.     $g_{opt}^c \leftarrow g^c, S_{opt}^c \leftarrow S_{\eta}^c$ 
15.  end if
16.   $\eta := \eta + 1$ 
17. end while
18. Compute the modulation signals (9).
19. Get the turn-on times of the firing signals according to Figure 3.
20. Apply the firing signals.

```

**Figure 3.** The PSM-PWM scheme for the CHB-based MMC phase ϕ .**3.3. Proposed PSM-PWM Strategy**

The classical model-based predictive control, after selecting the optimal vector $S_{\eta,opt}^{\phi}$, is applied during the whole sampling period producing an output voltage $v_{cr,\eta,opt}^{\phi}$. This solution produces an unbalanced switching frequency, causing, in turn, unbalanced stress on the power devices.

The proposed controller uses a modulation stage based on a phase shift multicarrier pulse-width modulation approach. A triangular three phase-shifted carrier signal with the same frequency and magnitude are needed to obtain the turn-on times of the firing signals of each cell using the proposed PSM-PWM strategy. The two adjacent carrier signals are shifted by $180^\circ/3$. By comparing one specific carrier signal $v_{cr,i}^{\phi}$ with a pair of inverted sinusoidal modulation signals, we obtain the firing signals of s_{x1}^{ϕ} and s_{x3}^{ϕ} , as shown in

Figure 3. Note that the carrier frequency and the sampling frequency are the same, and the modulation signals are associated with the optimal phase voltages and are normalized between -1 and 1 , that is:

$$v_{cont}^{\phi} = \frac{v_{cN,opt}^{\phi}}{3v_{dc}}. \quad (9)$$

3.4. Theoretical Results

A parametric analysis was performed to evaluate the performance of the proposed controller. For that purpose, different sampling frequencies (from 15 kHz to 35 kHz in 1 kHz steps) and current amplitude references (from 1 A to 6 A in 0.5 A steps) were considered. The performance of the proposed controller was analyzed in steady-state operation, considering the mean square error phase current i_c^d tracking as a figure of merit. Figure 4a shows the parametric MSE evolution, where it is observed that at low reference current amplitudes, the mean square error levels remained practically invariant as a function of the sampling frequency variation (from 0.071 A for 15 kHz to 0.068 A for 35 kHz). However, as the reference current became higher, the efficiency of the controller in terms of the lower root mean square error improved. For the particular case of $i_c^d = 6$ A, the MSE was reduced from 1.107 A (for 15 kHz) to 0.085 A (for 35 kHz of sampling frequency). Figure 4b summarizes in a level curve the different MSE values obtained in the parametric analysis.

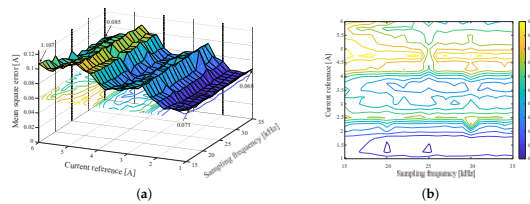


Figure 4. Phase current (i_c^d) tracking analysis after the change in reference amplitude from 1 A to 6 A and sampling frequency from 15 kHz to 35 kHz. (a) Parametric i_c^d mean square error evolution. (b) Level curves of the parametric MSE analysis.

4. Experimental Assessment

The proposed 7-level CHB-based MMC was validated through experimental results obtained by using a custom test bench, as shown in Figure 5. This converter was implemented using three cells per phase arranged in a cascade scheme. Each cell integrated four SiC-MOSFET semiconductor devices and was fed with an independent dc-link voltage. The dc-link voltages were implemented using independent linear dc sources, which ensured the balance in the dc-link level voltages of the multilevel converter. The 7-level converter was controlled by a real-time platform based on dSPACE MicroLabBox programmed using a MATLAB/Simulink environment considering a $T_s = 25 \mu s$ sampling time. The frequency at the grid side was 50 Hz, and the voltage was set to 310.2 V. The rest of the electrical parameters used for the controller were $v_{dc} = 33$ V, $R_f = 0.09 \Omega$, $L_f = 3$ mH, $R_L = 23.2 \Omega$, and $L_L = 55$ mH. The active power and current tracking measurements were performed with analogue meters and were used as a figure of merit to validate the proposed control strategy.

Initially, the 7-level CHB-based MMC was analyzed in an open-loop configuration. Figure 6 shows the 7 levels of the output voltage (v_c^d) and the load current (i_L^d) evolution at the output of the multilevel converter. Then, the FSF-MPC controller was evaluated in a closed-loop to analyze the current control's performance at the load side under transient conditions. Figure 7a shows the current tracking evolution when a reference amplitude changed from 0.5 A to 1 A. The result showed excellent and fast-tracking of its reference.

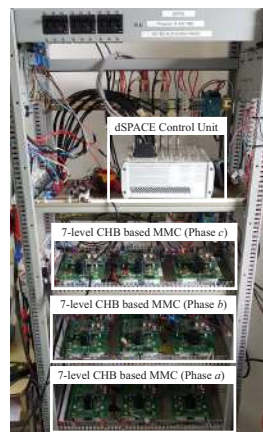


Figure 5. The 7-level CHB-based MMC experimental test bench including the dSPACE platform and the protection devices.

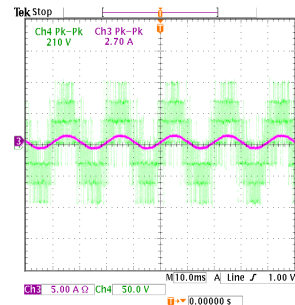


Figure 6. Voltage at the output of the 7-level CHB-based MMC (before the filter) and load current (i_L^0).

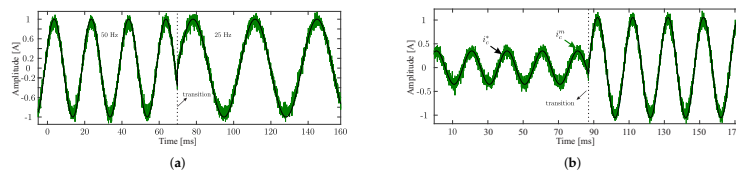


Figure 7. Phase current (i_c^0) tracking analysis under transient conditions. (a) Phase current (i_c^0) tracking analysis after the change in reference amplitude from 0.5 A to 1 A. (b) Phase current (i_c^0) tracking analysis after the change in reference frequency from 50 Hz to 25 Hz.

Then, the system's dynamic response was verified by measuring the output response when having a variation in the frequency of reference current from 50 Hz to 25 Hz. It can

be verified from Figure 7b that the current had the amplitude and frequency specified by the reference current, which shows the proper operation of the 7-level CHB-based MMC and the implemented current control. The mean square error (MSE) was around 0.08 A in both cases. Similar results were observed for phases *b* and *c* and are not been included for conciseness. On the other hand, the 7-level CHB-based MMC was evaluated from the point of view of active power control at the load side. In this test, a multi-step active power reference (P_L^*) was defined considering $Q_L^* = 0$ Var. Figure 8 shows the results of the reactive power tracking. As shown, the active power applied to the load followed its reference. Finally, Figure 9a shows the simulation results of the load current total harmonic distortion (THD) profile. As observed from the results, the proposed controller provided low ripples as well as a good harmonics profile at the load current side (around 2.16%). The theoretical results are consistent with the harmonic profile obtained experimentally. According to Figure 9b, the experimental load side current THD was around 3.76 %. Note that an analytical comparison of the proposed control technique against other state-of-the-art methods will be not discussed in this paper and is beyond the scope of the article.

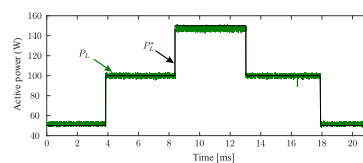


Figure 8. Multistep active power reference tracking analysis.

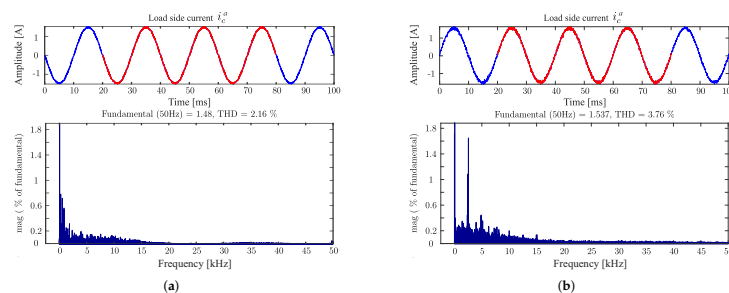


Figure 9. Load side phase current (i_c^a) THD analysis. (a) Simulation results. Load side current (upper) and THD measurements (lower). (b) Experimental results. Load side current (upper) and THD measurements (lower).

5. Conclusions

The paper described the implementation of a 7-level CHB-based MMC and implemented a model-based predictive control strategy. The feasibility and effectiveness of the overall system were investigated and validated through experimental results under steady-state and transient conditions. The controller used a phase shift multicarrier pulse-width modulation strategy. Among the advantages of the proposed FSF-MPC control strategy are: (a) the better harmonic profile of the load phase currents minimizing the total harmonic distortions at the load side; (b) good dynamics performance in terms of the MSE in the tracking reference currents. It can be noted that due to the simple nature of the implemented controller, it could be performed in any industrial application of a wide range of power.

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Abbreviations

The following abbreviations have been employed in this work:

AC	Alternating current
CHB	Cascade H-Bridge
FSF	Fixed switching frequency
IGBT	Isolated Gate Bipolar Transistors
MMC	Modular multilevel converter
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MPC	Model-based predictive control
PCC	Point of common coupling
PSM-PWM	Phase shift multicarrier PWM
PWM	Pulse-width modulation
SiC	Silicon Carbide
THD	Total harmonic distortion
VSCs	Voltage source converters

Nomenclature

C_{dc}	dc-link capacitor
g_a, g_b, g_c	FSF-MPC cost functions
i_L^a, i_L^b, i_L^c	Load phase currents
i_c^a, i_c^b, i_c^c	Converter phase currents
$\hat{i}_c^a(k+1), \hat{i}_c^b(k+1), \hat{i}_c^c(k+1)$	Converter phase current predictions
i_{ca}, i_{cb}	MMC currents in the $\alpha - \beta$ subspace
$i_c^{a*}, i_c^{b*}, i_c^{c*}$	Converter phase current references
v_c^a, v_c^b, v_c^c	Converter phase voltages
n_c	Number of cells
P_c^*	Instantaneous active power reference
Q_c^*	Instantaneous reactive power reference
Q_L	Instantaneous reactive load power
T	Clarke's transformation matrix
x	Corresponding cell number
y	Switching device in each cell
T_s	Sampling time
v_{dc}	dc-link voltage
R_f	Filter resistance
L_f	Filter inductance
$S_{\eta, opt}^{\phi}$	Optimum vector
$v_{c, \eta, opt}^{\phi}$	Optimal voltage
$v_{cr, x}^{\phi}$	Carrier wave
v_{cont}^{ϕ}	Modulation signals

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Article

Harmonics Compensation by Using a Multi-Modular H-Bridge-Based Multilevel Converter

Raul Gregor , Julio Pachter , Alejandro Espinoza, Alfredo Renault , Leonardo Comparatore 
and Magno Ayala 

Laboratory of Power and Control Systems (LSPyC), Facultad de Ingeniería, Universidad Nacional de Asunción, Luque 2060, Paraguay; jpachter@ing.una.py (J.P.); aespinoza@fiuna.edu.py (A.E.); arenault@ing.una.py (A.R.); lcomparatore@ing.una.py (L.C.); mayala@ing.una.py (M.A.)

* Correspondence: rgregor@ing.una.py; Tel.: +595-981813164

Abstract: This paper presents an active power filter based on a seven-level cascade H-bridge where the main contribution is a control strategy that combines model-based predictive control, the voltage vectors of the converter output levels, the phase shift PWM technique, and suboptimal DC-link voltage control. The proposed scheme greatly simplified the overall control system, making it well suited to compensate the current harmonics distortion at the grid side, generated by nonlinear loads connected to the point of common coupling. In addition, the proposed method achieved a balancing of the capacitor voltages of the seven-level cascade H-bridge converter by using the minimum DC-link voltage sensors. This feature significantly reduced the control system complexity and provided a low computational burden. Experimental results confirmed the feasibility and effectiveness of the proposed controller.

Keywords: harmonics compensation; multilevel converter; multimodular APF



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1. Introduction

Currently, power quality issues play an increasingly important role in AC power distribution systems due to the complex electric scenario, where different kinds of dynamic loads such as power converters, AC motor drives, and distributed energy resources (DERs) are integrated. From a practical point of view, a power quality problem can be defined as the deviation of the magnitude and frequency from the ideal sinusoidal waveform [1,2]. These power quality problems have given rise to different developments, and these problems have been addressed in the literature from complementary aspects, depending on the type of compensation. Among these mitigation techniques used for power quality issues in the distribution system, it is possible to find the custom power devices (CPDs) based on the active power filter (APF), commonly used for reactive power compensation, harmonic mitigation, and balancing of source currents [3,4]. Additional devices such as the dynamic voltage restorer (DVR) are used to compensate unbalanced voltage disturbance [5,6], and unified power quality conditioners (UPQCs) are used to compensate both voltage and current quality problems [7,8].

Moreover, in power quality applications, regardless of the implemented compensation system, the voltage source converters (VSCs) are considered a fundamental element of the compensation systems [9,10]. A conventional two-level VSC has so far been the most widely used converter in APFs; however, it creates a poor harmonic profile, leading to additional power quality and loss issues [11,12]. In recent years, the multilevel converter (more than two levels) has drawn the attention of researchers, and the literature has reported the development of APFs based on a multilevel converter injecting current at the point of common coupling (PCC) in order to achieve the desired reactive power compensation with high-quality waveforms. Regarding the multilevel converter topology, the cascade H-bridge (CHB) is currently one of the greatest topologies due to its advantages, such as

the modular converter topology (which simplifies the increase in the number of levels of the converter), and it does not require a very large number of clamping diodes or flying capacitors. Due to these advantages, the CHB APF is now considered as a very competitive topology in the new generation of reactive power compensation devices [13,14]. Commonly, the APF based on the CHB multilevel converter is designed using IGBT power electronics devices, but recently, silicon carbide (SiC) MOSFET devices have gained the focus of researchers because these devices can reach high switching frequencies, far higher than what could be achieved with a multilevel converter based on IGBTs, exhibiting higher blocking voltage, lower on-state resistance, and higher thermal conductivity, enabling better efficiency [15,16]. Nevertheless, for power quality applications using an active power filter, it is not enough to integrate fast switching devices. Rather, it is necessary to address this issue together with the control algorithm [17,18].

The control strategies implemented in the APF are the PID control techniques which need a large number of variables to be measured [19], the hysteresis control, which has a high band value, producing the greater propagation of low-order harmonic distortion and a low value [20], increasing switching losses, while model-based predictive control (MPC) is a nonlinear control technique applied to power converters [21,22], having some advantages such as fast dynamic response, the ability to handle multivariable systems [23], nonlinearities, and constraints. Some disadvantages are that it depends on the model of the system, and it uses a variable switching frequency, which causes the propagation of low-order harmonics in the output current that deteriorate the performance of the system [24]. On the other hand, the MPC applied to the APF based on seven-level cascade H-bridge converters uses the switching states, which correspond to a specific voltage level, which is normally a constant reference voltage [25], but having floating capacitors such as the DC-link, by which they are charged and discharged according to the polarity of the filter current, which generates ripples in the capacitor voltages. Therefore, there is an error propagation between the measured DC-link voltages with respect to their reference value [26,27].

The main contribution of this work is the implementation of an MPC technique that combines the selection of the optimal seven-level converter output voltage vectors (VVs) together with the phase-shifted PWM (PSPWM) approach. On the other hand, the proposed control strategy combines a suboptimal solution in order to achieve the DC-link voltage balance, simplifying the control structure and the experimental test bench.

In this regard, the proposed control method optimizes the prediction model using the estimates of the DC-link voltages in combination with the iterations of the control to obtain the sign of the output voltages of each CHB, thus avoiding using a constant reference voltage. In addition, a control is added that regulates the voltages of the DC-link capacitors to the reference values, minimizing the number of DC-link voltage controllers.

The proposed control technique was tested under different operating points, considering transient and steady-state conditions. The rest of the paper is organized as follows. The next section introduces the proposed multimodal APF topology. In the same section, the three-phase seven-level CHB converter scheme is analyzed, and the mathematical model of the APF based on the three-phase seven-level converter is extracted. Subsequently, the predictive model, the DC-link voltage controller, and the modulation strategy are presented in the same section. Section 3 describes the experimental test bench. In Section 4, the experimental results are shown, in which two figures of merit are used as a reference, the current tracking and harmonics compensation. Finally, in Section 5, the conclusions of the work are given.

2. Multimodal APF Model

Figure 1 shows the control scheme applied to the multimodal APF based on the 7-level 3-phase CHB multilevel converter. Note that each cell of the CHB has an independent DC-link and four switching devices based on the SiC-MOSFET semiconductors. The 7-level 3-phase converter topology is implemented by connecting three cells in series per phase.

Then, 36 firing signals, represented by $S_{xy}^\phi \in \{0, 1\}$, are used to control each cell, ϕ being the phase ($\phi = a, b$, or c), x the cell number in each phase ($x = 1, 2, 3$), and y the switching device in each cell ($y = 1, 2, 3$, or 4). Table 1 shows a combination of the firing signals taking phase “a” as an example in order to generate 7 voltage levels at the output of the 7-level converter. A similar analysis can be extended to other phases considering allowable combinations and avoiding short circuits in the DC-link of each cell.

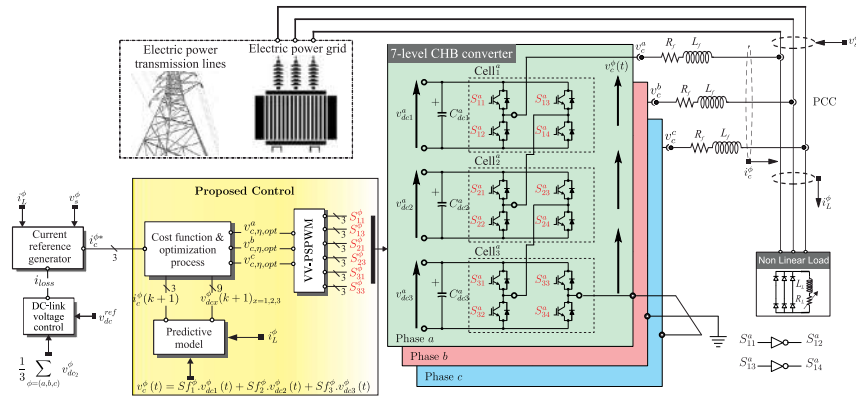


Figure 1. Proposed control scheme for the multimodular APF.

Table 1. Voltage vectors.

S_{η}^{ϕ}						η	$v_{c,\eta}^{\phi}$
Cell $_1^{\phi}$		Cell $_2^{\phi}$		Cell $_3^{\phi}$			
S_{11}^{ϕ}	S_{13}^{ϕ}	S_{21}^{ϕ}	S_{23}^{ϕ}	S_{31}^{ϕ}	S_{33}^{ϕ}		
0	1	0	1	0	1	1	$-3 \cdot v_{dc}^{\phi}$
0	1	0	1	0	0	2	$-2 \cdot v_{dc}^{\phi}$
0	1	0	0	0	0	3	$-1 \cdot v_{dc}^{\phi}$
0	0	0	0	0	0	4	$0 \cdot v_{dc}^{\phi}$
1	0	0	0	0	0	5	$1 \cdot v_{dc}^{\phi}$
1	0	1	0	0	0	6	$2 \cdot v_{dc}^{\phi}$
1	0	1	0	1	0	7	$3 \cdot v_{dc}^{\phi}$

To obtain an equation that describes the dynamics of the converter output voltage, the switching function of the CHB multilevel converters Sf_x is used. This is derived for each phase and H-bridge cell as:

$$Sf_x^\phi = S_{x1}^\phi \cdot S_{x4}^\phi - S_{x2}^\phi \cdot S_{x3}^\phi \quad (1)$$

The value of Sf_x^ϕ indicates the charging and discharging among the DC-link capacitors C_{dc1}^ϕ , C_{dc2}^ϕ , and C_{dc3}^ϕ . Supposing the current i_c^ϕ flows from the converter to the grid, then the capacitor C_{dcx}^ϕ is charging if $Sf_x^\phi = -1$, discharging if $Sf_x^\phi = 1$, and unchanged if $Sf_x^\phi = 0$. The output voltage of the multilevel converter depends on the switching function and the voltage in each of the DC-link capacitors and can be expressed as:

$$v_c^\phi(t) = Sf_1^\phi \cdot v_{dc1}^\phi(t) + Sf_2^\phi \cdot v_{dc2}^\phi(t) + Sf_3^\phi \cdot v_{dc3}^\phi(t) \quad (2)$$

The values of v_{dc1}^ϕ , v_{dc2}^ϕ , and v_{dc3}^ϕ are the estimated voltages of each DC-link previously filtered. They may not be equal to their reference voltage due to the dynamics of the system.

According to Kirchhoff's law for the DC side and considering the ideal case ($R_{dc} = \infty$, where R_{dc} is a resistor that concentrates the overall losses in the DC side), the currents flowing into the electrical grid from capacitors C_{dc1}^ϕ , C_{dc2}^ϕ , and C_{dc3}^ϕ , whose capacitance values $C_{dcx}^\phi = C_{dc}$, can be expressed as:

$$i_{Cx}^\phi(t) = C_{dc} \cdot \frac{d(v_{dcx}^\phi)}{dt} = S f_x^\phi \cdot i_c^\phi \quad (3)$$

On the other hand, the proposed controller is based on the explicit APF mathematical model in order to calculate the effects of control actions over the evolution of the state variables. The dynamics of the system's model can be obtained by using Kirchhoff's circuit laws. Notice that the APF based on the CHB 7-level converter is connected at the PCC. Next, by applying Kirchhoff's laws for the AC side of the APF and using (2) and (3), assuming the currents flow from the converter to the electrical grid, the following equations in the state-space representation are obtained for each phase:

$$\begin{bmatrix} \dot{i}_c^\phi(t) \\ \dot{v}_{dc1}^\phi(t) \\ \dot{v}_{dc2}^\phi(t) \\ \dot{v}_{dc3}^\phi(t) \end{bmatrix} = \mathbb{F} \cdot \begin{bmatrix} i_c^\phi(t) \\ v_{dc1}^\phi(t) \\ v_{dc2}^\phi(t) \\ v_{dc3}^\phi(t) \end{bmatrix} + \mathbb{G} \cdot \begin{bmatrix} v_s^\phi(t) \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (4)$$

where $v_s^\phi(t) \forall \phi \in \{a, b, c\}$ are the grid voltages and $i_c^\phi(t)$ and $v_{dc}^\phi(t)$ are the APF output currents and voltages, respectively. The matrices $\mathbb{F}$ and $\mathbb{G}$ are:

$$\mathbb{F} = \begin{bmatrix} -\frac{R_f}{L_f} & \frac{S f_1^\phi}{L_f} & \frac{S f_2^\phi}{L_f} & \frac{S f_3^\phi}{L_f} \\ \frac{S f_1^\phi}{C} & 0 & 0 & 0 \\ \frac{S f_2^\phi}{C} & 0 & 0 & 0 \\ \frac{S f_3^\phi}{C} & 0 & 0 & 0 \end{bmatrix} \quad (5)$$

$$\mathbb{G} = \begin{bmatrix} -\frac{1}{L_f} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \quad (6)$$

R_f being the parasitic (series) resistance of the inductive filter L_f connected between the output of the multilevel converter and the PCC.

3. Predictive Model

The predictive model can be obtained from (4) by using a forward-Euler discretization method. Euler's method is the most basic explicit method for numerical integration of ordinary differential equations and consequently carries a low computational burden, which benefits the experimental implementation [28–30]. The APF discrete-time model is given by:

$$\begin{bmatrix} \hat{i}_c^\phi(k+1) \\ \hat{v}_{dc1}^\phi(k+1) \\ \hat{v}_{dc2}^\phi(k+1) \\ \hat{v}_{dc3}^\phi(k+1) \end{bmatrix} = \mathbb{A} \cdot \begin{bmatrix} i_c^\phi(k) \\ v_{dc1}^\phi(k) \\ v_{dc2}^\phi(k) \\ v_{dc3}^\phi(k) \end{bmatrix} + \mathbb{B} \cdot \begin{bmatrix} v_s^\phi(k) \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (7)$$

where:

$$\mathbb{A} = \begin{bmatrix} \left(1 - \frac{R_f T_s}{L_f}\right) & \frac{T_s S f_1^\phi}{L_f} & \frac{T_s S f_2^\phi}{L_f} & \frac{T_s S f_3^\phi}{L_f} \\ \frac{T_s S f_1^\phi}{C} & 1 & 0 & 0 \\ \frac{T_s S f_2^\phi}{C} & 0 & 1 & 0 \\ \frac{T_s S f_3^\phi}{C} & 0 & 0 & 1 \end{bmatrix} \quad (8)$$

$$\mathbb{B} = \begin{bmatrix} -\frac{T_s}{L_f} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \quad (9)$$

T_s being the sampling time.

3.1. Current Reference Generation

The proposed controller requires the calculation of the reference currents in order to evaluate the cost function in (18). Figure 2 illustrates the block diagram of the current reference calculation based on synchronous reference frame (SRF) theory. As can be seen from Figure 2, the current reference generation block diagram requires the measurement of the capacitor voltages, load currents, and source voltages. The phase currents and voltages are represented in the $d-q-0$ subspace by using Park's transformation matrix:

$$\mathbb{T}_{dq} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos(\theta) & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ -\sin(\theta) & -\sin(\theta - \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \quad (10)$$

The use of a three-phase PLL is required to synchronize these signals with the source voltages. Due to the nonlinear loads, the components $d-q$ can be decomposed into two elements, one DC component $\bar{i}_{LdDC}$ associated with the 50 Hz fundamental frequency power and the other one $\bar{i}_{Ld}$ associated with the harmonic frequencies. The currents in the d and q axes can be represented as the sum of their fundamental and harmonic components as follows:

$$\begin{aligned} i_{Ld} &= \bar{i}_{LdDC} + \bar{i}_{Ld} \\ i_{Lq} &= \bar{i}_{Lq} + \bar{i}_{Lq} \end{aligned} \quad (11)$$

The DC component of the current $\bar{i}_{LdDC}$ is separated using a digital second-order low-pass filter (LPF), as shown in the scheme of Figure 2. The reference currents in the time domain, based on the references i_{cd}^* , i_{cq}^* , and i_{c0}^* , are:

$$\begin{bmatrix} i_c^* \end{bmatrix} = [\mathbb{T}_{dq}]^{-1} \cdot \begin{bmatrix} i_{cd}^* \\ i_{cq}^* \\ i_{c0}^* \end{bmatrix} \quad (12)$$

where:

$$i_{cd}^* = i_{Ld} - \bar{i}_{LdDC} - i_{loss} \quad (13)$$

$$i_{cq}^* = i_{Lq} \quad (14)$$

The term i_{loss} in (13) is the additional power needed to increase the average voltage across the DC-link capacitors and to balance the losses of the 7-level CHB converter associated with the switching states. This current i_{loss} is obtained by using a PI controller.

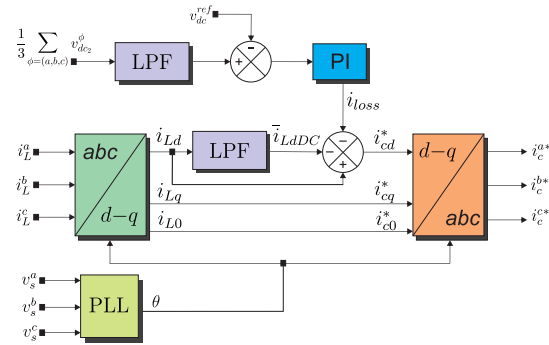


Figure 2. Current reference generation based on SRF theory including the DC-link voltage controller.

3.2. DC-Link Voltage Control

Depending on how the filter injects current into the electrical power grid, the DC-link capacitors release or absorb energy, causing a drop or increase, respectively, in the v_{dc}^ϕ voltage of the capacitors. On the other hand, semiconductor losses by switching and conduction also cause a reduction of the capacitor voltages. That is why a regulation system is needed that maintains the voltage levels at a certain average reference value. To regulate the average capacitor voltages to reference values in the CHB 7-level converter, a common methodology is based on the measurement of each capacitor voltage in order to evaluate the error to implement a PI controller in discrete-time [31,32]. This procedure represents an optimal solution to the capacitor voltage regulation process; however, it increases the complexity of the overall system, especially when considering the multilevel converter. A different approach is based on the modification of the cost function of predictive control, including a term that seeks to achieve the capacitor voltages' balance by applying an optimal switching function at each sampling period [33,34].

In this work, a suboptimal solution was proposed combining both approaches. The implemented DC-link voltage controller is shown in Figure 3. As can be seen from Figure 3, the voltage measurements performed made only in the middle cell. These capacitor voltages are used in the predictive model block to predict their voltage level, and an average of these measurements is used to calculate the voltage error applied to the PI control block, through an LPF. According to [35], an approximation to the proportional (kp) and integral (ki) gain values can be written as:

$$e_k^\phi = v_{dc}^{ref} - v_{dc2}^\phi \quad (15)$$

$$i_{loss}^\phi = i_{loss(k-1)} + kp \cdot (e_k^\phi - e_{k-1}^\phi) + Tm_{pi.ki} \cdot e_k^\phi \quad (16)$$

$$i_{loss} = \frac{1}{3} \sum_{\phi=a,b,c} i_{loss}^\phi \quad (17)$$

$$k_p = \frac{C_{dc}}{2 \cdot T_c} \quad (17)$$

$$k_i = \frac{k_p}{2}$$

where e_k^ϕ represents the error between the reference and the previously filtered measured voltages v_{dc2}^ϕ , then the loss current i_{loss} is calculated, $i_{loss(k-1)}$ being the loss current estimated in the previous instant, $e_{(k-1)}$ the voltage error calculated in the previous instant,

Tm_{pi} the PI controller actuation time, and finally, i_{loss} , which represents the sum of the loss currents of each phase with respect to the middle cell.

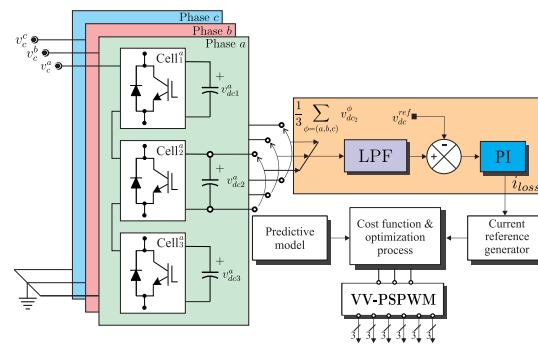


Figure 3. Block diagram of the DC-link voltage control scheme.

3.3. Cost Function and Optimization Process

The proposed controller was based on model-based predictive control to follow the current references and simultaneously achieve a balance in the capacitor voltages. The MPC was based on the optimization process in which a cost function is minimized. This cost function is defined as the difference between the reference values and the estimates obtained through the prediction model. In the three-phase control scheme, a general cost function is defined for each phase, which includes the reference current tracking error and the voltage tracking error for the capacitors, which are independently evaluated using the following equation:

$$g^\phi = \| i_c^\phi - \hat{i}_c^\phi(k+1) \|^2 + \lambda \| v_{dc}^{ref} - \hat{v}_{dc}^\phi(k+1) \|^2 \quad (18)$$

where λ is a weight factor in the optimization process.

Next, the optimization algorithm selects the optimum vector $S_{\eta,opt}^\phi$ for each firing signal of each cell by the evaluation and minimization of the predefined multi-objective cost function represented by (18). Algorithm 1 summarizes the optimization process.

3.4. Voltage Vectors' Phase-Shifted PWM Strategy

After selecting the optimal vector $S_{\eta,opt}^\phi$, which corresponds to an optimal voltage $v_{c,\eta,opt}^\phi$ given by (2), the classic solution is to apply this output voltage during one sampling period. However, the proposed method uses a modulation stage based on the phase-shifted pulse width modulation (PSPWM) approach. Three phase-shifted triangular carrier waves (with the same frequency and magnitude peak-to-peak) are needed to obtain the turn-on times of the firing signals of each cell. The phase-shift between the two adjacent carriers is $180^\circ/3$. By comparing one specific carrier wave $v_{tr,x}^\phi$ with a pair of inverted modulation signals v_{cont}^ϕ and $-v_{cont}^\phi$, we obtain the firing signals of s_{x1}^ϕ and s_{x3}^ϕ , as shown in Figure 4. Note that the carrier frequency is equal to the sampling frequency, and the modulation signals are normalized between -1 and 1 . The modulated signals are associated with the optimal voltages as:

$$v_{cont}^\phi = \frac{v_{c,\eta,opt}^\phi}{3v_{dc}^{ref}}. \quad (19)$$

Algorithm 1 Optimization algorithm.

```

1 Initialize  $g_{opt}^a := \infty, g_{opt}^b := \infty, g_{opt}^c := \infty, \eta := 0$ 
2 Compute the APF current references (12).
3 while  $\eta \leq 7$  do
4    $S_{\eta}^{\phi} \leftarrow S_{xy}^{\phi} \forall x \text{ \& } y = 1, 2, 3$ 
5   Compute the output voltage of the multilevel converter (2).
6   Calculate the APF prediction currents and voltage (4).
7   Compute the cost function (18).
8   if  $g^a < g_{opt}^a$  then
9      $g_{opt}^a \leftarrow g^a, S_{\eta,opt}^a \leftarrow S_{\eta}^a$ 
10  end if
11  if  $g^b < g_{opt}^b$  then
12     $g_{opt}^b \leftarrow g^b, S_{\eta,opt}^b \leftarrow S_{\eta}^b$ 
13  end if
14  if  $g^c < g_{opt}^c$  then
15     $g_{opt}^c \leftarrow g^c, S_{\eta,opt}^c \leftarrow S_{\eta}^c$ 
16  end if
17   $\eta := \eta + 1$ 
18 end while
19 Compute the modulation signals (19).
20 Obtain the turn-on times of the firing signals according to Figure 4.
21 Apply the firing signals.

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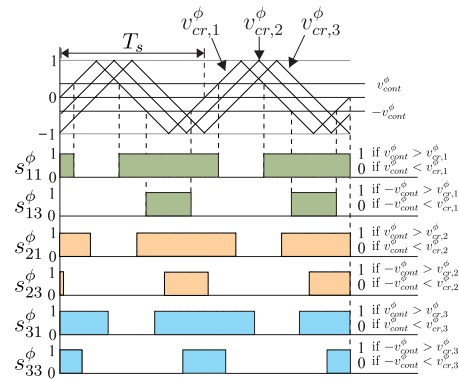


Figure 4. PSPWM waveform generation.

4. Experimental Test Bench

The multimodular APF built for experimental validation is shown in Figure 5. The test bench integrated three individual CHB cells per phase, interconnected in series. Control signals were conditioned in independent driver boards and were transmitted from the control board to the drivers by using fiber optics in order to avoid electromagnetic noises from the switching devices in the control signals. The control board was based on the dSPACE MicroLabBox multipurpose control system. The power semiconductor devices used were SiC-MOSFETs from Cree, CAS120M12BM2, with 120 A and 1200 V maximum drain–source current and drain–source voltage, respectively.

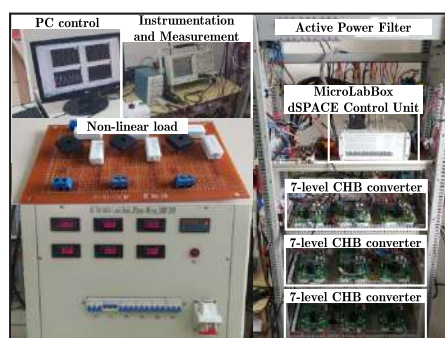


Figure 5. Experimental test bench.

In order to apply the proposed controller, analog phase voltages and currents were measured using a multimodular PCB. The analog signals were digitized by using the dSPACE MicroLabBox analog-to-digital converter (ADC) modules with 16 bit resolution. Figure 5 shows the current and voltage measurement boards designed to obtain the electrical variables necessary for the implementation of the control algorithms. The sampling frequency was 18 kHz, which was the same as the equivalent switching frequency, and the carrier frequency for PWM modulation was 1 kHz.

5. Experimental Validation

In order to verify the performance of the proposed APF, this section shows the experimental results considering $v_g^0 = 120$ Vrms, $v_{dc}^{ref} = 75$ V, $L_f = 10$ mH. The nonlinear load was a three-phase rectifier. The DC side of the bridge rectifier was connected to an RL load with $R_L = 100 \Omega$, 50Ω , 25Ω , and $L_L = 114$ mH, respectively. The capacitance of the DC-link in all DC cells (C_{dc}) was $20,000 \mu\text{F}$. The defined cost function in (18) with $\lambda = 0.02$ was selected to evaluate the performance of the proposed controller, prioritizing the current tracking as the first control objective and the DC-link tracking voltage as the second objective.

5.1. Verification of the Harmonics Compensation

The harmonics compensation performance was tested by using a nonlinear load under different grid current conditions. The experimental results of the total harmonic distortion (THD) were obtained by using the data captured with the control desk software of the dSPACE MicroLabBox. Load currents (i_L), APF output currents (i_c), grid currents (i_s), as well as source voltages (v_s) and DC-link (V_{dc}) voltages were captured and analyzed. Figure 6 shows the THD level in the grid side before compensation considering three operating points $R_L = 100 \Omega$, 50Ω , and 25Ω , respectively. Under these operating conditions, the THD of the currents at the grid side was 29.36%, 27.37%, and 28.33%, respectively. Once the APF was connected, the compensation process started. The output APF currents (i_c) were injected at the PCC in order to compensate the harmonics distortion at the grid side. According to the grid currents' evolution shown in Figure 6, after connecting the APF, currents at the grid side (i_s) quickly became sinusoidal. The THD level in the grid currents decreased to the values of 4.75%, 5.25%, and 6.6%, respectively, for each load impedance value. A significant improvement in terms of harmonic compensation was observed.

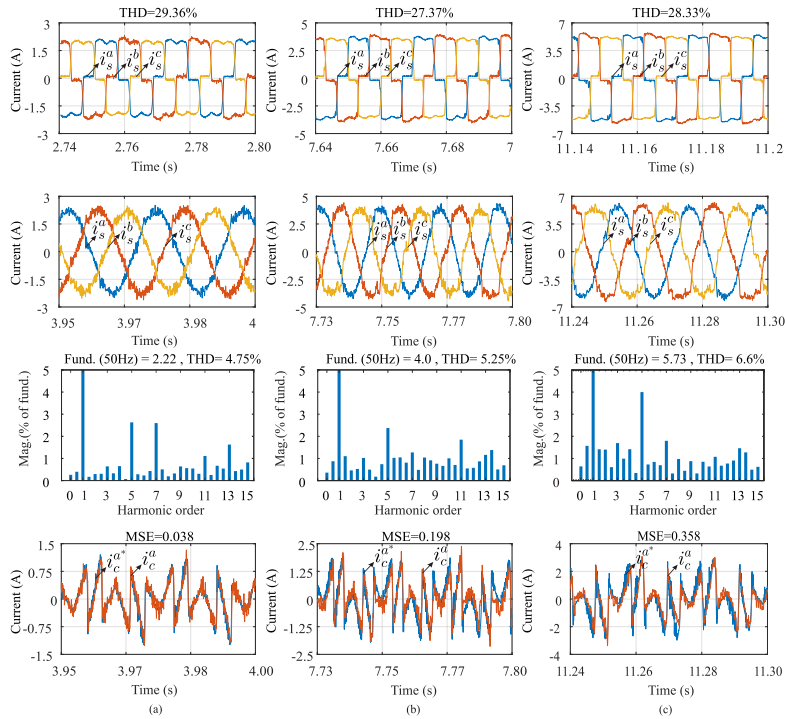


Figure 6. Experimental results of source current harmonics compensation at the grid side considering a nonlinear load and three operating points: (a) $R_L = 100 \, \Omega$, (b) $R_L = 50 \, \Omega$, and (c) $R_L = 25 \, \Omega$.

To quantify the performance of the proposed MPC based on the PSPWM algorithm, the mean-squared error (MSE) between the reference currents calculated by (12) and the measured current captured by the ADC of the dSPACE MicroLabBox were used as the figure of merit. According to the results shown in Figure 6, the MSE increased as the load power increased, being able to quantify in 0.038A, 0.198A, and 0.358A, respectively. On the other hand, Figure 7a shows the source current evolution (i_s^g) at the grid side. It shows the distortions due to the high level of THD existing in the electrical grid due to the nonlinear load connected at the PCC. Once the APF was enabled, the current injection (i_s^d) at the PCC was produced by the APF in order to compensate the harmonics distortion of the source current, as shown in Figure 7b, where the CHB seven-level converter output voltage (v_c^d) is also shown. From Figure 7c, once the harmonics compensation process starts, a significant decrease can be observed in the THD level existing in the source current at the grid side (i_s^g).

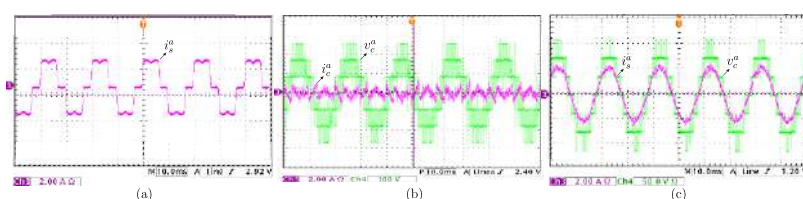


Figure 7. Steady operation of the APF (a) uncompensated source current, (b) compensated source current and filter output voltage, and (c) voltage and current APF output.

In order to analyze the APF behavior under dynamic conditions, a load resistance (R_L) variation from $150\ \Omega$ to $50\ \Omega$ was applied. Figure 8a presents the dynamic behavior of the APF current injection (i_c^a) at the PCC in order to produce the harmonics compensation at the grid side (i_s^a) where the measured grid current rapidly rose to the nominal value without oscillations that may affect the stability of the system. On the other hand, Figure 8b shows the dynamic behavior of the APF output voltage (v_c^a) produced by the load resistance variation. It can be seen how from the transient condition, the duty cycle of the APF output voltage was modified in order to generate a current compensation (i_c^a) with greater amplitude injected at the PCC, resulting in a compensated current at the grid side (i_s^a) with a low harmonic content, even instantaneously after the transient condition.

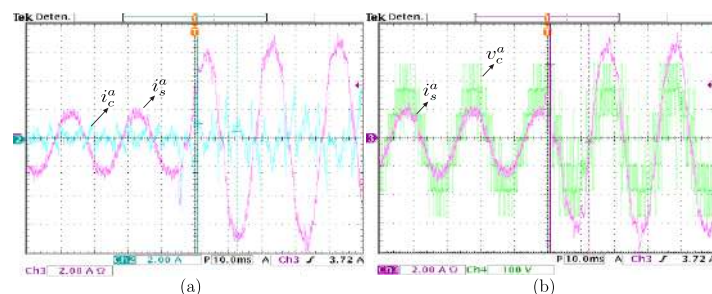


Figure 8. Transient behavior of the APF (a) current i_c^a and i_s^a for increased load and (b) current i_s^a and voltage v_c^a for instantaneous load resistance changes.

5.2. Verification of the DC-Link Voltage Control

In order to verify the effects of the DC-link voltage control under the transient condition, the APFs were intentionally disabled during the steady-state. After three seconds, the APF was suddenly connected, causing a transient in the DC-link voltages. Figure 9a shows the experimental waveforms of capacitor voltages under transient conditions. According to the experimental results, the PI control implemented on three cells was enough to achieve the stable behavior of the DC-link voltages. Once the APF was enabled, the capacitor voltages converged to their reference value. Figure 9b shows the harmonics compensation in the source current at the grid side when the APF was connected at the PCC. The experimental results demonstrated in Figures 6–9 confirmed the feasibility and effectiveness of the proposed controller.

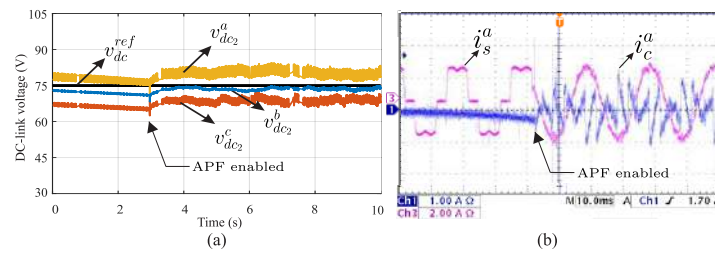


Figure 9. Transient behavior of the APF (a) DC-link voltage control performance and (b) source current harmonics compensation.

5.3. Verification of the Compensation for Unbalanced Voltages

Main currents may be unbalanced if nonlinear loads or AC source voltages are unbalanced. Figure 10a shows the measured phase voltage waveforms for the unbalanced grid voltages and nonlinear load conditions. The voltage amplitude unbalance was 20% for the experiment. Under these operating conditions, the active power filter operated properly, reducing the harmonic distortions at the grid side, as shown in Figure 10b.

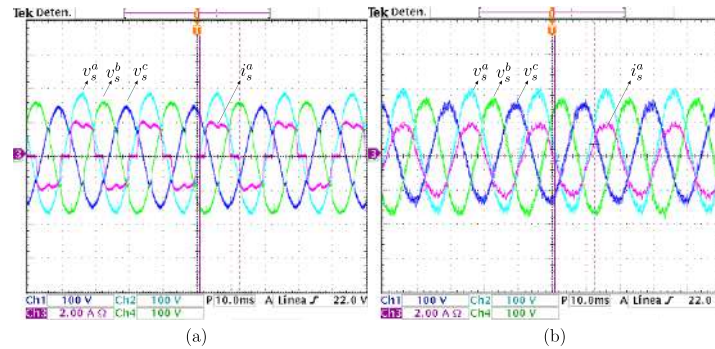


Figure 10. Unbalanced voltages (a) uncompensated by the source current and (b) compensated by the source current.

6. Conclusions

This paper presented the implementation of a multimodular H-bridge SiC-MOSFET-based APF using a simple and novel controller combining the concepts of model-based predictive control, voltage vector PSPWM, and suboptimal DC-link voltage control. The feasibility and effectiveness of the overall system was investigated and validated through experimental results. In this regard, the proposed system proved to be viable to compensate the current harmonics distortion at the grid side generated by nonlinear loads. The fifth and seventh harmonics originally present in the grid currents, with 27.30% of the THD value, were compensated after the interconnection of the APF at the PCC. The reduction of the THD of the grid currents from 27.30% to 4.75% proved the quality of the power system would be enhanced. This characteristic was evaluated under different operating points. The controller was found to be effective, and its validity was demonstrated based on the experimental results through the analysis of the MSE in the tracking reference currents obtained by the SRF theory, under both steady-state and dynamic conditions. From the

point of view of the harmonics compensation of the current at the grid side, the proposed algorithm showed a good dynamic response even under transient operating regimes and unbalanced voltages.

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Abbreviations

The following abbreviations were employed in this work:

AC	Alternating current
ADC	Analog-to-digital converter
APF	Active power filter
CHB	Cascade H-bridge
CPDs	Custom power devices
DC	Direct current
DERs	Distributed energy resources
DVR	Dynamic voltage restorer
IGBT	Isolated gate bipolar transistors
LPF	Low-pass filter
MOSFET	Metal–oxide–semiconductor field-effect transistor
MPC	Model predictive control
MSE	Mean-squared error
PCB	Printed circuit board
PCC	Predictive current control
PI	Proportional–integral
PLL	Phase-locked loop
PSPWM	Phase-shifted PWM
PWM	Pulse width modulation
SiC	Silicon carbide
SRF	Synchronous reference frame
THD	Total harmonic distortion
UPQC	Unified power quality conditioners
VSCs	Voltage source converters
VV	Voltage vectors

Nomenclature

ϕ	Phase of power grid a , b , and c
S_{xy}^ϕ	Firing signals
x	Corresponding cell number
y	Switching device in each cell

C	Capacitor
v_{dc}^{ϕ}	Voltages measured in the DC-link
v_c^{ϕ}	Converter voltage output
i_c^{ϕ}	Current estimation in the capacitor
i_c^{ϕ}	APF measured current
i_l^{ϕ}	Load measured current
i_s^{ϕ}	Power grid measured current
v_s^{ϕ}	Voltage measurement in the power grid
R_f	Filter resistance
L_f	Filter inductance
$i_c^{\phi}(k+1)$	APF current prediction
$v_{cx}^{\phi}(k+1)$	APF voltage prediction
T_s	Sample time
v_{dc}^{ref}	DC-link voltage reference
i_{ld}	Active power load in synchronous frame
i_{lq}	Reactive power load in synchronous frame
i_{ldDC}	continuous component of i_{ld}
i_{ld}	alternating component of i_{ld}
i_{cds}	Active power reference in synchronous frame
i_{cq*}	Reactive power reference in synchronous frame
θ	Phase angle calculated by the PLL
i_{loss}	Estimation of the current required to charge the capacitors
T_{dq}	Transformation matrix a, b, c to $d - q$
T_{dq}^{-1}	Inverse transformation matrix $d - q$ to a, b, c
$i_c^{\phi*}$	Reference current of phases a, b, and c.
e_k^{ϕ}	Error between the reference and measured voltages
e_{k-1}^{ϕ}	Voltage error calculated in the previous instant
i_{loss}^{a+b+c}	Sums of the loss currents of each phase
$i_{loss(k-1)}$	Loss current calculated in the previous instant
T_{mpi}	PI controller actuation time
k_p	PI proportional constant
k_i	PI integral constant
$S_{\eta,opt}^{\phi}$	Optimum vector
$v_{c,\eta,opt}^{\phi}$	Optimal voltage
$v_{cr,x}^{\phi}$	Carrier wave
v_{cont}^{ϕ}	Modulation signals

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Experimental Validation of the DSTATCOM Based on SiC-MOSFET Multilevel Converter for Reactive Power Compensation

Raúl GREGOR*

Julio PACHER*

Alfredo RENAULT*

Leonardo COMPARATORE*

Jorge RODAS*

*Laboratory of Power and Control Systems, Facultad de Ingeniería, Universidad Nacional de Asunción
Luque, CP 2060, Paraguay

E-mail: {rgregor, jpacher, arenault, lcomparatore & jrodas}@ing.una.py

ABSTRACT

Power quality problems are associated, among other things, with the reactive power generated at the AC side in distribution systems. In this regard, the three-phase distribution static compensator is actually becomes a viable alternative in order to achieve reactive power compensation or in other words to obtain a unity power factor. This paper introduces the experimental validation of the distribution static compensator based on a 7-level cascade H-Bridge converter. The experimental test bench is based on the silicon carbide metal-oxide-semiconductor field-effect transistor devices. The results are obtained by using a fixed switching frequency model-based predictive controller based on a pulse-width modulation strategy. The proposed design is implemented to mitigate power quality issues induced by reactive load and experimental results are provided to show the performance of the proposed controller.

Keywords: Predictive control, active power filter, cascaded H-Bridge multilevel converter, reactive power compensation.

NOMENCLATURE

CPDs	Custom power devices.
DSTATCOM	Distribution static compensation.
DVR	Dynamic voltage restorer.
CHB	Cascade H-Bridge.
MPC	Model predictive control.
THD	Total harmonic distortion.
C_{dc}	dc-link capacitor.
g_a, g_b, g_c	FCS-MPC cost functions.
i_s^a, i_s^b, i_s^c	Power grid phase currents.
i_L^a, i_L^b, i_L^c	Load phase currents.
i_c^a, i_c^b, i_c^c	DSTATCOM phase currents.
$\hat{i}_c^a, \hat{i}_c^b, \hat{i}_c^c$	DSTATCOM phase current predictions.
$i_c^{a*}, i_c^{b*}, i_c^{c*}$	DSTATCOM phase current references.
v_c^a, v_c^b, v_c^c	DSTATCOM phase voltages.

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n_c	Number of cells.
P_c^*	Instantaneous active power reference.
Q_c^*	Instantaneous reactive power reference.
Q_L	Instantaneous reactive load power.
$\mathbf{T}$	Clarke's transformation matrix.
T_s	Sampling time.
V_{dc}	dc-link voltage.

1. INTRODUCTION

For today's AC power distribution system, power quality problems play an increasingly important role. This is mainly due to the growth of the electricity demand in the residential and industrial sectors. Recently, poor power quality has become a more important issue for both power suppliers and customers. From a practical point of view, a power quality problem can be defined as a deviation of magnitude and frequency from the ideal sinusoidal waveform. This deviation usually affects both voltage and currents in the distribution systems. These power quality problems have given rise to different developments and these problems have been addressed in the literature from complementary aspects, depending on the type of compensation. Among these developments using for mitigation of power quality issues in the distribution system, it is possible to find the custom power devices (CPDs) based on distribution static compensation (DSTATCOM) are commonly used for reactive power compensation, harmonic mitigation and balancing of source currents [1],[2]. Additional devices such as a dynamic voltage restorer (DVR) is used to compensate unbalance voltage disturbance and a unified power quality conditioners (UPQCs) is used to compensate both, voltage and current quality problems [3],[4]. Moreover, in power quality applications, regardless of the implemented compensation system, the voltage source converters (VSCs) are considered a fundamental element of the compensation systems. A conventional two-level VSC has so far been the most widely used converter in DSTATCOMs however it creates a poor harmonic profile, leading to additional power quality and loss issues [5],[6]. In recent years, the multilevel converter (more than two-level) has drawn the attention of

researchers and the literature has reported the development of DSTATCOMs based on multilevel converter injecting current at the point of common coupling (PCC) in order to achieve the desired reactive power compensation [7],[8]. Regarding the multilevel converter topology, the cascade H-Bridge (CHB) is currently one of the greatest topologies due to its advantages, such as the modular converter topology (which simplifies the increase in the number of levels of the converter) and it does not require a very large number of clamping diodes or flying capacitors [9]. Due to these advantages, the CHB DSTATCOM is now considered as a very competitive topology in the new generation of reactive power compensation devices [10]. Commonly the DSTATCOM based on CHB multilevel converter has been designed using IGBTs power electronics devices but, recently, the SiC-MOSFET devices have gained the focus of researchers because these devices can reach high switching frequencies, far higher to what could be achieved with a multilevel converter based on IGBTs [11],[12]. Nevertheless, for power quality applications using an active power filter, it is not enough to integrate fast switching devices. Rather it is necessary to address this issue together with the control algorithm. In this regard, this paper presents the experimental validation of DSTATCOM based on the SiC-MOSFET CHB multilevel converter for reactive power compensation. This technology uses a fixed switching frequency model-based predictive controller (FSF-MPC) based on a pulse-width modulation strategy [13],[14]. The rest of the paper is divided as follows. Next section introduces the proposed DSTATCOM topology. In the same section, the three-phase 7-level CHB converter scheme is analyzed and the mathematical model of the DSTATCOM based on three-phase 7-level converter and load are extracted. In section 3, the proposed FSF-MPC strategy is detailed. In section 4, the experimental results are shown in which two figures of merits were used as a reference, the current tracking, and reactive power compensation. Finally, in section 5, conclusions of the work are given.

2. PROPOSED DSTATCOM TOPOLOGY

Fig. 1 shows the 7-level three-phase CHB multilevel converter. Notice that each cell of the CHB has an independent dc-link and four switching devices based on the SiC-MOSFETs [15]. The 7-level three-phase converter topology is implemented connecting three cells in series per phase. Then, thirty-six firing signals, represented by S_{xy}^{ϕ} are used to control each cell, being ϕ the phase ($\phi = a, b$ or c), x the cell number in each phase and y the switching device in each cell ($y = 1, 2, 3$ or 4). Table I shows some combination of the firing signal taking phase “a” as an example in order to generate seven voltage levels at the output of the 7-level converter. A similar analysis can be extended to other phases considering allowed combinations and avoid short circuits in the dc-link of each cell.

On the other hand, the control scheme of the proposed FSF-MPC for the DSTATCOM is shown in Fig. 2. This controller is based on the explicit DSTATCOM mathematical model in order to calculate the effects of control actions over the evolution of the states. The dynamic of the system’s model can be obtained by using Kirchhoff’s circuit laws. Notice that the DSTATCOM based on the CHB 7-level converter is connected at the PCC. Next, by applying Kirchhoff’s laws for the AC side of the DSTATCOM, the following equations in the state-space representation are obtained:

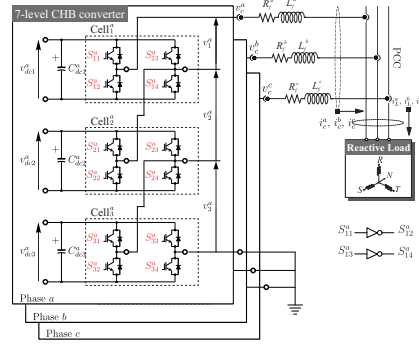


Fig. 1. Three-phase 7-level cascade H-Bridge multilevel converter.

TABLE I
POSSIBLE COMBINATIONS OF ACTIVATION SIGNALS

S_{xy}^a						η	$v_{c,\eta}^a$
Cell ^a ₁₁	Cell ^a ₁₂	Cell ^a ₂₁	Cell ^a ₂₂	Cell ^a ₃₁	Cell ^a ₃₂		
0	0	0	0	0	0	1	$0 \cdot v_{dc}^a$
0	0	0	0	0	1	2	$-1 \cdot v_{dc}^a$
0	0	0	0	1	0	3	$1 \cdot v_{dc}^a$
.	.	.	.	.	.	.	.
0	1	0	1	0	0	21	$-2 \cdot v_{dc}^a$
0	1	0	1	0	1	22	$-3 \cdot v_{dc}^a$
.	.	.	.	.	.	.	.
1	0	1	0	1	0	43	$3 \cdot v_{dc}^a$
.	.	.	.	.	.	.	.
1	0	1	0	1	1	44	$2 \cdot v_{dc}^a$
.	.	.	.	.	.	.	.

$$\begin{bmatrix} \dot{i}_c^a(t) \\ \dot{i}_c^b(t) \\ \dot{i}_c^c(t) \end{bmatrix} = \mathbb{F} \cdot \begin{bmatrix} i_c^a(t) \\ i_c^b(t) \\ i_c^c(t) \end{bmatrix} + \mathbb{G} \cdot \begin{bmatrix} v_s^a(t) - v_c^a(t) \\ v_s^b(t) - v_c^b(t) \\ v_s^c(t) - v_c^c(t) \end{bmatrix} \quad (1)$$

where

$$\mathbb{F} = \begin{bmatrix} -\frac{R_f}{L_f} & 0 & 0 \\ 0 & -\frac{R_f}{L_f} & 0 \\ 0 & 0 & -\frac{R_f}{L_f} \end{bmatrix}, \quad \mathbb{G} = \begin{bmatrix} \frac{1}{L_f} & 0 & 0 \\ 0 & \frac{1}{L_f} & 0 \\ 0 & 0 & \frac{1}{L_f} \end{bmatrix} \quad (2)$$

being R_f the parasitic (series) resistance of the inductive filter L_f connected between the output of the multilevel converter and the PCC.

A. DSTATCOM predictive model

The predictive model can be obtained from (1) by using a forward-Euler discretization method. Euler’s method is the most basic explicit method for numerical integration of ordinary differential equations and consequently carries a low computational burden that benefits the experimental implementation. The DSTATCOM discrete-time model is given by:

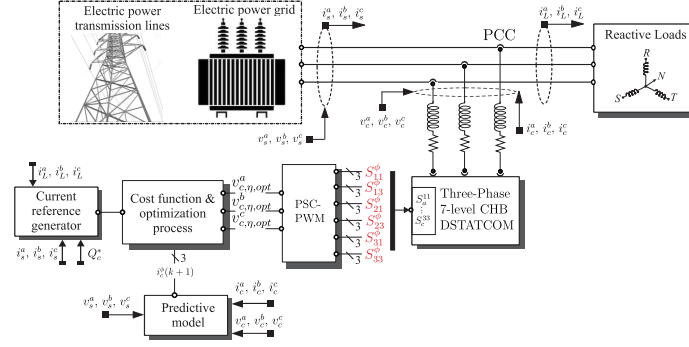


Fig. 2. Control scheme of the proposed FSF-MPC DSTATCOM.

$$\begin{bmatrix} \hat{i}_c^a(k+1) \\ \hat{i}_c^b(k+1) \\ \hat{i}_c^c(k+1) \end{bmatrix} = \mathbb{A} \begin{bmatrix} i_c^a(k) \\ i_c^b(k) \\ i_c^c(k) \end{bmatrix} + \mathbb{B} \begin{bmatrix} v_s^a(k) - v_c^a(k) \\ v_s^b(k) - v_c^b(k) \\ v_s^c(k) - v_c^c(k) \end{bmatrix} \quad (3)$$

where

$$\mathbb{A} = \begin{bmatrix} a_1 & 0 & 0 \\ 0 & a_1 & 0 \\ 0 & 0 & a_1 \end{bmatrix}, \quad \mathbb{B} = \begin{bmatrix} \frac{T_s}{L_f} & 0 & 0 \\ 0 & \frac{T_s}{L_f} & 0 \\ 0 & 0 & \frac{T_s}{L_f} \end{bmatrix} \quad (4)$$

being $a_1 = \left(1 - \frac{R_f T_s}{L_f}\right)$ and T_s the sampling time.

B. Current reference generation

The proposed FSF-MPC requires the prior calculation of the reference currents in order to evaluate the cost function in (9). For simplicity, the phase currents and voltages are represented in the $\alpha - \beta$ subspace by using Clarke's transformation matrix:

$$\mathbf{T} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}. \quad (5)$$

Then, the current references in $\alpha - \beta$ subspace in function of active and reactive power are:

$$\begin{bmatrix} i_{c\alpha}^* \\ i_{c\beta}^* \end{bmatrix} = \frac{1}{(v_{s\alpha})^2 + (v_{s\beta})^2} \begin{bmatrix} v_{s\alpha} & v_{s\beta} \\ v_{s\beta} & -v_{s\alpha} \end{bmatrix} \begin{bmatrix} P_c^* \\ Q_c^* \end{bmatrix}. \quad (6)$$

In order to achieve unity power factor on the grid side, it must be ensured that $P_c^* = 0$. This condition implies that the DSTATCOM does not absorb active power. On the other hand, the instantaneous reactive power reference can be written as:

$$Q_c^* = -Q_L = v_{s\alpha} i_{L\beta} - v_{s\beta} i_{L\alpha} \quad (7)$$

where Q_L is compensated by the CHB DSTATCOM system. The DSTATCOM phase currents references used in the optimization process are:

$$\begin{bmatrix} i_{c\alpha}^{a*} \\ i_{c\alpha}^{b*} \\ i_{c\alpha}^{c*} \end{bmatrix} = \mathbf{T}^{-1} \begin{bmatrix} i_{c\alpha}^* \\ i_{c\beta}^* \\ 0 \end{bmatrix}. \quad (8)$$

C. Cost function and optimization process

The proposed controller is based on the model predictive current control. The MPC is based on the optimization process in which a cost function is minimized. This cost function is defined as the difference between reference currents and the predicted currents obtained through the prediction model. In the three-phase control scheme, the cost functions are evaluated independently from the following equations:

$$\begin{aligned} g^a &= \|i_c^{a*} - \hat{i}_c^a(k+1)\|^2 \\ g^b &= \|i_c^{b*} - \hat{i}_c^b(k+1)\|^2 \\ g^c &= \|i_c^{c*} - \hat{i}_c^c(k+1)\|^2. \end{aligned} \quad (9)$$

Next, the optimization algorithm selects the optimum vector $S_{\eta,opt}^{ab}$ for each firing signal of each cell by the evaluation and minimization of the predefined cost function represented by (9). To make the thing clearer, Algorithm 1 summarizes the optimization process.

Algorithm 1 Optimization algorithm of the proposed modulated FSF-MPC current controller

1. Initialize $g_{opt}^a := \infty, g_{opt}^b := \infty, g_{opt}^c := \infty, \eta := 0$
2. Compute the STATCOM current references (8).
3. **while** $\eta \leq \varepsilon$ **do**
4. $S_{\eta}^a \leftarrow S_{xy}^a \forall x \& y = 1, 2, 3$
5. Calculate the STATCOM prediction currents (3).
6. Compute the cost function, (9).
7. **if** $g^a < g_{opt}^a$ **then**
8. $g_{opt}^a \leftarrow g^a, S_{opt}^a \leftarrow S_{\eta}^a$
9. **end if**
10. **if** $g^b < g_{opt}^b$ **then**
11. $g_{opt}^b \leftarrow g^b, S_{opt}^b \leftarrow S_{\eta}^b$
12. **end if**
13. **if** $g^c < g_{opt}^c$ **then**
14. $g_{opt}^c \leftarrow g^c, S_{opt}^c \leftarrow S_{\eta}^c$
15. **end if**
16. $\eta := \eta + 1$
17. **end while**
18. Compute the modulation signals (10).
19. Get the turn-on times of the firing signals according to Fig. 3.
20. Apply the firing signals.

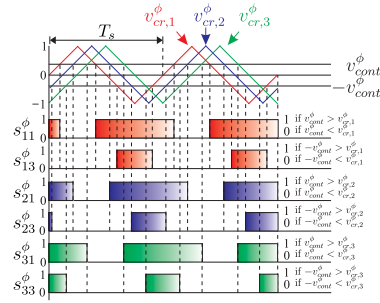


Fig. 3. PSC-PWM scheme for CHB DSTATCOM phase ϕ .

3. PROPOSED FSF-MPC STRATEGY

After selecting the optimal vector $S_{\eta,opt}^\phi$, which corresponds to an optimal voltage $v_{c,\eta,opt}^\phi$, the classic solution is to apply this output voltage during the whole sampling period. However, the proposed method uses a modulation stage that consists in a phase shift multicarrier pulse width modulation (PSC-PWM). Three phase-shifted triangular carrier waves (with the same frequency and magnitude peak to peak) are needed to obtain the turn-on times of the firing signals of each cell. The phase-shift between the two adjacent carriers is $180^\circ/3$. By comparing one specific carrier wave $v_{cr,i}^\phi$ with a pair of inverted modulation signals v_{cont}^ϕ and $-v_{cont}^\phi$, we obtain the firing signals of s_{x1}^ϕ and s_{x3}^ϕ , as shown in Fig. 3. Note that the carrier frequency is equal to the sampling frequency and the modulation signals are associated with the optimal phase voltages and are normalized between -1 and 1, that is:

$$v_{cont}^\phi = \frac{v_{c,\eta,opt}^\phi}{3v_{dc}}. \quad (10)$$

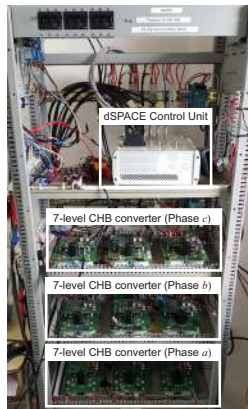


Fig. 4. Block diagram of the DSTATCOM test bench including the 7-level CHB converter, the dSPACE platform and the protection devices.

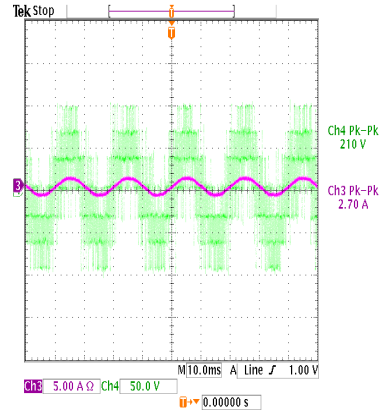


Fig. 5. Voltage at the output of the 7-level converter (before the filter) and load current (i_L^ϕ).

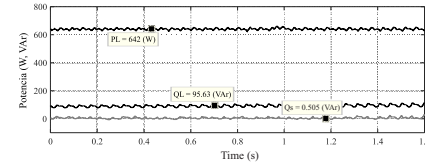


Fig. 6. Experimental result of the reactive power compensation.

4. EXPERIMENTAL VALIDATION

The proposed DSTATCOM topology is validated through experimental results obtained by using a custom test bench. This latter integrates three H-Bridge cells per phase that cascaded each other. Each cell is fed with an independent dc-link and integrates four SiC-MOSFET semiconductor devices. The DSTATCOM is controlled by a dSPACE MicroLabBox real-time platform considering a $T_s = 25 \mu s$ sampling time. The proposed controller is developed by using a MATLAB/Simulink environment. The grid frequency and voltage are set to 50 Hz and 310.2 V, respectively. Other electrical parameters are $v_{dc} = 33$ V, $R_f = 0.09 \Omega$, $L_f = 3$ mH, $R_L = 23.2 \Omega$ and $L_L = 55$ mH. The experimental measurements of voltage and current are performed with analog meters and are used to validate the proposed control strategy.

Initially, the 7-level CHB converter is analyzed in an open-loop configuration. Fig. 5 shows the seven levels of voltages at the output of the 7-level CHB converter and the load current (i_L^ϕ) evolution. Then, the 7-level CHB DSTATCOM is connected at the PCC to perform a dynamic test for the reactive power compensation at the grid side. Fig. 6 shows the results of reactive power compensation. In this test, the active and reactive power at the load side are $Q_L = 95.6$ VAR and $P_L = 642$ W, respectively. As shown in Fig. 6 the reactive power at the grid side is close to zero $Q_S = 0.5$ VAR after the DSTATCOM integration. The reactive power compensation is also verified in Fig. 7 where it shows a unit power factor after the reactive power compensation

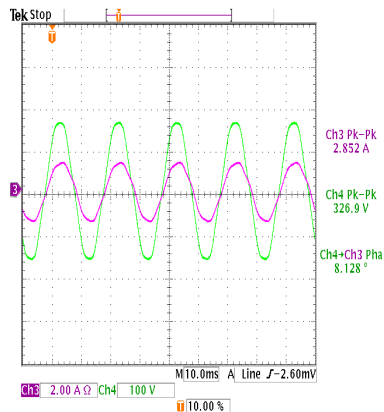


Fig. 7. Voltage (v_g^a) and current (i_g^a) at the grid side with unit power factor after the reactive power compensation.

at the grid side. This is a zero degree phase shift between the grid voltage (v_g^a) and grid current (i_g^a). Similar results have been obtained for phases b and c and have not been included for the sake of conciseness.

5. CONCLUSION

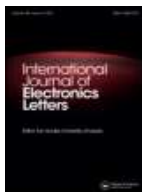
This paper performs experimental validation of the DSTATCOM based on SiC-MOSFET 7-level converter connected to the point of common coupling in order to maintain nearly unit power factor even when reactive loads are connected to the grid. To accomplish this a control strategy has been proposed based on a fixed switching frequency model-based predictive controller in conjunction with the pulse-width modulation strategy. In this regard, the proposed control scheme fixes the switching frequency from the sampling frequency, which causes a balance in the switching losses in all semiconductor devices. On the other hand, the capability of the 7-level converter has been verified by using the experimental DSTATCOM test bench and it is found to be efficient and robust which is validated through performance under nominal operation, in reactive power compensation.

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Efficiency analysis of a modular H-bridge based on SiC MOSFET

Julio Cesar Pacher Vega^a, Jorge Esteban Rodas Benitez ^a,
Raul Igmarr Gregor Recalde ^a, Marco Rivera ^b, Alfredo Renault Lopez^a
and Leonardo David Comparatore Franco^a

^aLaboratory of Power and Control Systems, Facultad de Ingeniería, Universidad Nacional de Asunción, San Lorenzo, Paraguay; ^bFaculty of Engineering, Universidad de Talca, Curico, Chile

ABSTRACT

Several new high-performance power semiconductors have appeared during the last decade, being the silicon carbide (SiC) MOSFETs the most promising to be commercialised as an alternative of Si IGBT. This paper presents the performance analysis of a controller for a full H-bridge based on SiC MOSFET technology used for high frequency and medium voltage applications. The switching performance of a modular H-bridge is analysed and the efficiency/losses and temperature dissipation are experimentally measured in order to help engineers to design and develop circuits using this power semiconductor. A comparison between SiC MOSFET and Si MOSFET is also presented.

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1. Introduction

Silicon carbide (SiC) MOSFETs have been attracted as a superior alternative for power switching devices because they offers several advantageous electrical characteristics such as lower on-resistance, higher temperature durability, higher speed switching performance and lower switching losses compared to Si IGBT (Mukunoki et al., 2016). These features allow the use of SiC MOSFETs for the development of more efficient systems that have been applied in recent years in many applications such as matrix converters (Safari, Castellazzi, & Wheeler, 2014), multilevel converters (Wu, Qin, Saeedifard, Wasynczuk, & Shenai, 2015), inverters (Gurpinar & Castellazzi, 2016) and DC/DC converters (Nakakohara et al., 2016). To exploit the features of the SiC MOSFET devices, the designers must know the technical limitations of the SiC MOSFET because the efficiency of the power devices have a very significant impact on the performance of the final system implemented. For example, a high switching frequency produces lower total harmonic distortion values, however the negative effect is that the switching power losses increase significantly at high frequencies. The ability to operate at high switching frequencies with reduced switching power losses is one of the features that differentiate SiC MOSFET from other mass-use switching devices.

CONTACT Julio Cesar Pacher Vega  jpacher@ing.una.py  Laboratory of Power and Control Systems, Facultad de Ingeniería, Universidad Nacional de Asunción, Paraguay San Lorenzo, Paraguay

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Although published results show the interest of the use of *SiC* MOSFET devices in several applications, they do not present a detailed performance analysis of the device (Tanabe et al., 2015, June; Yin, Tseng, Simanjorang, & Tu, 2017). Few comparative study between *SiC*-MOSFET and IGBT can be found in (Trentin, de Lillo, Empringham, Wheeler, & Clare 2015; Trentin et al., 2016) applying to matrix converters. In this context, the main contribution of this paper is the experimental efficiency/losses and thermographic analysis of the power device *SiC* MOSFET, using a modular H-bridge as a case study. Furthermore, a comparison between *SiC* MOSFET and *Si* MOSFET is also presented.

2. Description of the full H-bridge topology and experimental system

The block diagram of the H-bridge is shown in Figure 1(a). The control signals for the H-Bridge scheme are sent by two fibre-optic links whose signals are processed by the HFBR-2521Z fibre optic receiver (Figure 1(b)). Then, the two electrical PWM signals are sent to a block in charge of generating the complementary $\overline{PWM}$ signals necessary for the control of each branch of the H-bridge. This circuit also implements the necessary dead time between each PWM and its complement $\overline{PWM}$, which is performed by using XOR 74HC86 gates and resistive and capacitive elements. The driver for *SiC* MOSFETs is implemented using the IR2110S integrated circuit, as shown in Figure 1(c). For the assembly of the power stage of the design, the *SiC* MOSFET SCH2080KE, shown in Figure 1(d) is used. In order to achieve the modularity of each H-bridge cell, they have their own independent power source (VCC_1 and VCC_2) implemented by the galvanically isolated DC/DC converter CC10-1212SF (Figure 1(e)).

Figure 2(a) shows the experimental platform used for the tests. An *RL* load with values of $R = 20 \Omega$ and $L = 10 \mu H$ was used for the analysis.

Voltage measurements were performed with a Tektronix P5210A voltage differential probe, while the currents were measured using a Tektronix TCPA300 current probe. A

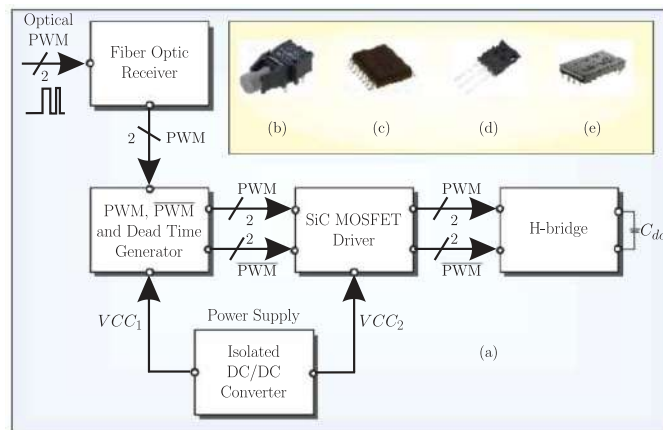


Figure 1. Block diagram of the H-bridge driver and its components.

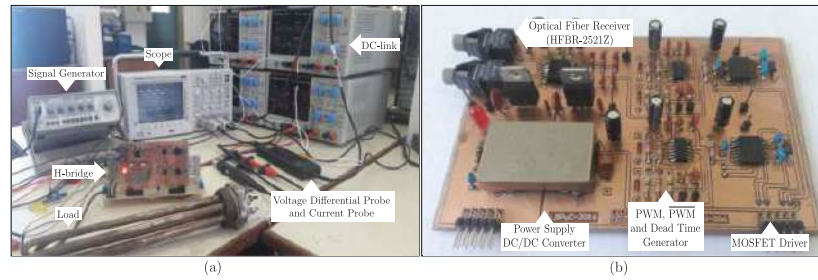


Figure 2. Experimental system: (a) measurement test rig setup, (b) H-bridge driver.

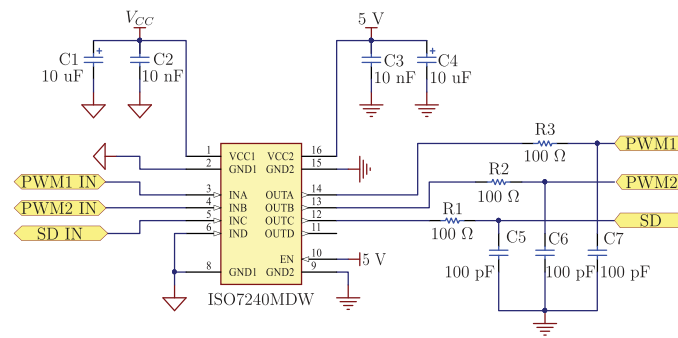


Figure 3. Conditioning circuit for PWM input signal with galvanic isolation and passive RC output filters.

variable DC-link was implemented by using several DC power sources Minipa model MPL-3305M, to capture the signals used a Tektronix digital oscilloscope model TDS3034C. The test signal was obtained from an EX Digital generator model FG-8002. Figure 2(b) shows the final design of the modular H-bridge.

Once the signal obtained by the fibre optic link has been processed, it is necessary to perform the conditioning of the PWM signal used to control the SiC-MOSFET shots, which signals are overlapping during high- or low-level transitions. The signal matching is implemented using the ISO7240 integrated circuit; these digital isolators have two isolated channels. Each isolation channel has a logic input and output buffer separated by a silicon dioxide insulation barrier (SiO₂). Used in conjunction with isolated power supplies, these devices prevent noise currents on a data bus or other circuit from entering the local reference and damaging or interfering with sensitive circuits. These devices have input thresholds with TTL levels and require two power voltages (3.3 V or 5 V). Figure 3 shows the circuit diagram designed to perform the conditioning of received PWM signals by using Altium Designer software.

3. Experimental results

Several experimental analyses were performed in order to analyse the modular H-bridge based on SiC MOSFET as well as a comparison with the same H-bridge but using a Si MOSFET. The diagram of the experimental platform implemented for the measurements is shown in Figure 4. The PWM signals are sent through the fibre optic link to the H-bridge controller, voltage and current measurements are made in the RL load, as well as measurements of the switching devices.

Figure 5 shows the PWM and $\overline{\text{PWM}}$ signals, where the dead time value is $1\ \mu\text{s}$ for a frequency $100\ \text{kHz}$. This dead time is obtained by a circuit composed of logic gates 74HC86 and resistive and capacitive elements. The output voltage (V_o) and output current (I_o) are shown in Figure 6. Note that I_o has a slower transitions between high and low levels compared with V_o due to the inductive nature of the load.

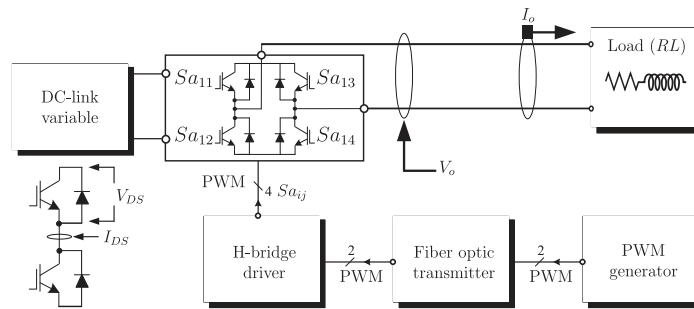


Figure 4. Diagram of the experimental platform implemented for the realisation of the measurements.

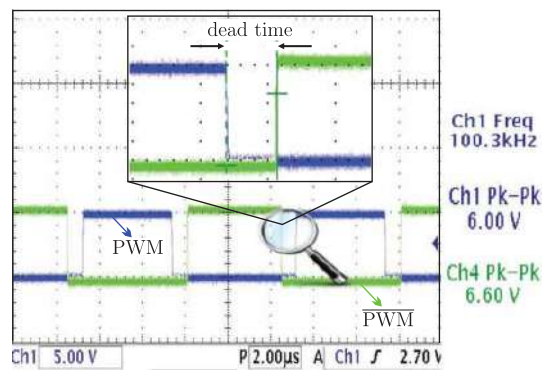


Figure 5. PWM and $\overline{\text{PWM}}$ signals and dead time (Ch1: PWM voltage–5 V/div; Ch2: $\overline{\text{PWM}}$ voltage – 5 V/div).

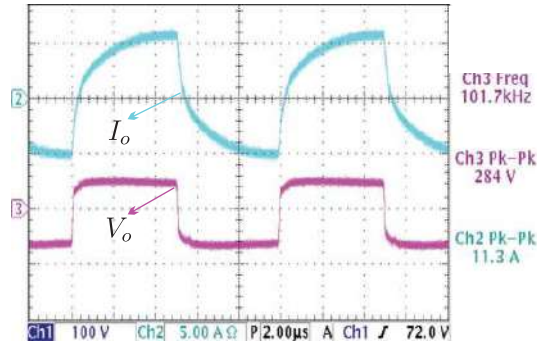


Figure 6. Output voltage (V_o) and output current (I_o) delivered to the RL load at 1 kW (Ch1: output voltage–100 V/div; Ch2: output current – 5 A/div).

In order to calculate the efficiency of the proposed modular full H-bridge the following equations are used for the conduction losses (Equation (1)) and switching losses (Equation (2)) presented by the SiC MOSFET (Wang et al., 2016):

$$P_{CM} = V_{DS} I_{Drms} = R_{DS(on)} I_{Drms}^2 \quad (1)$$

$$P_{sw} = \frac{V_{DD} I_D}{2} (t_{on} + t_{off}) f_s \quad (2)$$

being f_s the operating frequency, I_{Drms} the drain current root-mean squared (rms), $R_{DS(on)}$ the drain source resistance, V_{DD} the DC-link voltage, t_{on} and t_{off} the state transition time intervals, turn-on and turn-off, respectively. It is, therefore, necessary to measure the variables in equations (1) and (2) (see Figure 7).

Then, some tests have been carried out varying the output power (0.5 kW and 1 kW) as well as the switching frequency (from 50 kHz to 200 kHz). According to the obtained results (Figure 8), the global losses increase with frequency while the efficiency

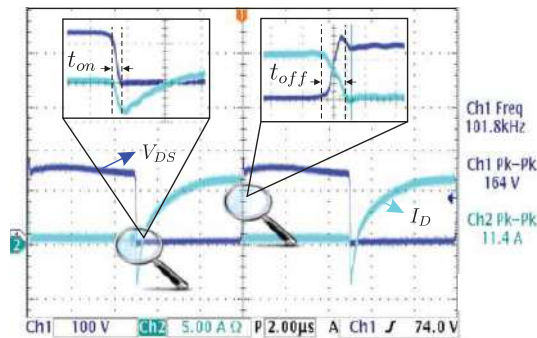


Figure 7. Modular H-bridge switching characteristics at 1 kW (Ch1: drain-source voltage – 100 V/div; Ch2: drain current – 5 A/div).

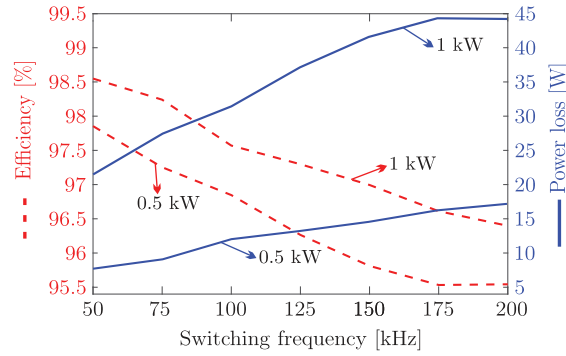


Figure 8. Efficiency (cut lines) and power losses (continuous lines) regarding the switching frequency.

decreases with the increase of the switching frequency. Notice that the efficiency is more than 95.5% for all analysed cases, being at 50 kHz the highest 98.5% efficiency for 1 kW of output power.

Then, it is interesting to make a thermal quantification of the *SiC* MOSFETs. Figure 9 shows a photograph obtained by a thermal imaging camera, being the temperatures on the *SiC* MOSFETs $SP_1 = 75.3^\circ\text{C}$, $SP_2 = 72.1^\circ\text{C}$, $SP_3 = 76.3^\circ\text{C}$, $SP_4 = 69.4^\circ\text{C}$. By a thermographic analysis it is possible to predict failure or malfunction points by non-uniform temperature as well as noting points of overheating. In this case the heating of each *SiC* MOSFET is approximately 7°C difference between the lower heating point with respect to greater heating. These measurements are important in determining the points of greatest stress with respect to the power dissipation in the modular H-bridge design.

To conclude the efficiency analysis, a comparative study between the *SiC* MOSFET and the Si MOSFET is performed. Some important specifications of both state-of-the-art power semiconductors are listed in Table 1. For this test, a DC current flowing in the

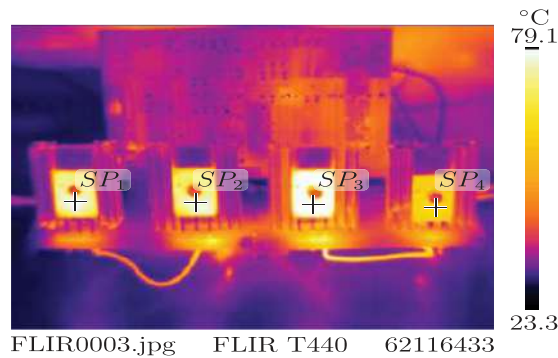
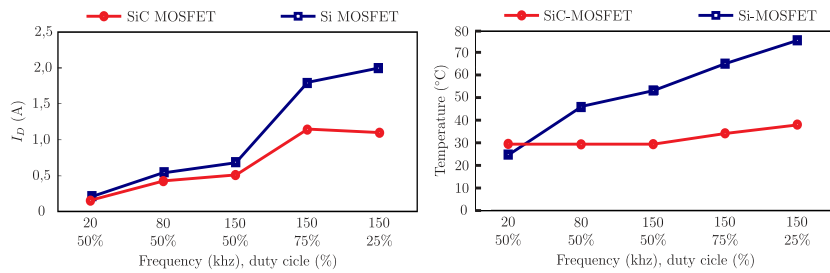


Figure 9. Thermographic image obtained from the H-bridge implemented with *SiC* MOSFETs.

Table 1. Specifications of SiC MOSFET and Si MOSFET.

Parameter	Unit	SiC-MOSFET	Si-MOSFET
Drain-to-source breakdown voltage	[V]	1 200	40
Static drain-to-source on-resistance	[mΩ]	80	1.4
Continuous drain current	[A]	40	195
Maximum power dissipation	[W]	262	375
Turn-on delay time	[ns]	37	65
Rise time	[ns]	33	827
Turn-off delay time	[ns]	70	97
Fall time	[ns]	28	355
Input capacitance	[pF]	1 850	10 315

**Figure 10.** Comparison between SiC MOSFET and Si MOSFET. (a) Drain current and (b) temperature analysis.

H-bridge driver is plotted in Figure 10(a) against PWM frequency and duty cycle. The red and blue lines indicate currents of SiC MOSFET and Si MOSFET H-bridge drivers, respectively. The load was the solar linear motor connected to each H-bridge driver by the same condition. Then the cause of the current difference is attributed to the device, where the Si MOSFET has less $R_{DS(on)}$ than the SiC MOSFET. As shown in Table 1, the response time of the SiC MOSFET is considerably lower than that of the Si MOSFET, whereby the SiC MOSFET develops lower power dissipation due to the switching losses. The currents at 150 kHz and with a duty cycle of 25 % is 1.1 A and 2.0 A for SiC MOSFET and Si MOSFET, respectively. Temperature rise of each device is plotted in Figure 10(b) similar to Figure 10(a). The temperature at 150 kHz and with a duty cycle of 25 % was 39°C and 76°C for SiC MOSFET and Si MOSFET, respectively. There is a big difference in temperature rise at high frequencies.

4. Conclusion

In this paper, the design and efficiency analysis of a modular H-bridge based on SiC MOSFET is presented. Experimental results show that the switching losses increase with frequency while conduction losses decrease with frequency. Switching losses in its transition from low to high represent the 92% of losses, while the transition from high to low represents the 2%. The conduction losses accounted for 6% of total losses. The design responds appropriately within the range of operating frequencies

ranging between 50 and 200 kHz, yielding an efficiency from 98% to 95% with increasing frequency. According to the experimental results for the comparison between SiC MOSFET with Si MOSFET by using normal H-bridge driver, temperature rise at high PWM frequencies was the most prominent difference between them. Considering that the PWM frequencies tested were 20 kHz up to 156 kHz and duty cycles were 25%, 50% and 75%, the highest temperatures were 39°C and 76°C for SiC MOSFET and Si MOSFET, respectively, both at PWM frequency of 150 kHz and duty cycle of 25%.

Disclosure statement

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ORCID

Jorge Esteban Rodas Benitez  <http://orcid.org/0000-0001-9732-704X>
 Raul Igmarr Gregor Recalde  <http://orcid.org/0000-0002-7717-4100>
 Marco Rivera  <http://orcid.org/0000-0002-4353-2088>

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Current control based on space vector modulation applied to three-phase H-Bridge STATCOM

A. Renault, M. Ayala, J. Pacher, L. Comparatore, R. Gregor, S. Toledo
Lab. of Power and Control Systems
Universidad Nacional de Asunción
Luque, Paraguay
{arenault, mayala, jpacher, lcomparatore, rgregor, stoledo}@ing.una.py

Abstract—This paper presents a modulated model predictive current control (MPC) based on space vector analysis applied to a three-phase H-Bridge STATCOM. This article proposes a modulation strategy, based on space vector modulation in $\alpha - \beta$ subspace, in order to mitigate the propagation of the THD of the current injected in the point of common coupling (PCC). Simulation results based are provided to quantify the performance, in terms of power RMS ripple and mean square error (MSE) of the measured phase currents and their corresponding references, of the proposed modulated predictive current control.

Index Terms—Active power filters, H-bridge converter, predictive current control, space vector modulation.

NOMENCLATURE

AC	Alternating current.
APF	Active power filter.
CHB	Cascade H-bridge.
DC	Direct current.
FCS-MPC	Finite-control-set model predictive control.
MSE	Mean square error.
PCC	Point of common coupling.
RMS	Root mean square.
STATCOM	Static var compensator.
SVM	Space vector modulation.
THD	Total harmonic distortion.
VSC	Voltage source converter.
C_{dc}	DC-link capacitor.
g_a, g_b, g_c	MPC cost functions.
i_s^a, i_s^b, i_s^c	Power grid phase currents.
i_L^a, i_L^b, i_L^c	Load phase currents.
i_c^a, i_c^b, i_c^c	STATCOM phase currents.
i_c^a, i_c^b, i_c^c	STATCOM phase current predictions.
$i_{c\alpha}, i_{c\beta}$	STATCOM currents in the $\alpha - \beta$ subspace.
$i_c^{a*}, i_c^{b*}, i_c^{c*}$	STATCOM phase current references.
v_c^a, v_c^b, v_c^c	STATCOM phase voltages.
n_c	Number of cells.
P_c^*	Instantaneous active power reference.
Q_c^*	Instantaneous reactive power reference.
Q_L	Instantaneous reactive load power.
$\mathbf{T}$	Clarke's transformation matrix.
T_s	Sampling time.
V_{dc}	DC-link voltage.

I. INTRODUCTION

The STATCOM are regulation devices based on VSCs and can absorb and transfer energy in the AC power transmission and distribution systems [1], [2]. STATCOMs are used to control the active and reactive power of the system, eliminate oscillations in the transmission line, regulate voltage, improve the system stability and reduce several transients [3]. One of the most attractive STATCOM topologies is the CHB, due to an excellent modularity in its configuration [4]–[7]. STATCOMs, based on H-bridge converters with SiC-MOSFET switching devices, have several advantages, such as the possibility of higher switching frequency, scalability and modular structure. Due to these advantages, they have been object of study and they are now considered a very competitive topology in the new type of STATCOM and can be applied to the electrical distribution power grid [8].

Several linear controllers are proposed for the CHB STATCOM [9], [10]. Recently, MPC has been presented in many power converters topologies, such as [11]–[14]. The advantages of MPC such as its simplicity and intuitiveness, high dynamic performance, multi-objective capabilities, suitability for nonlinear systems make it an interesting control strategy in power electronics applications [15]–[19]. Among the limitations of the MPC are the production of variable switching frequency which causes higher THD that propagates to the grid and causes curling [20], [21]. In that order, this document proposes a combination between a modulation strategy, based on SVM, and a PCC strategy applied to the three-phase STATCOM, in such a way to compensate the reactive power and reduce the curling effect of the currents filter by managing a fixed switching frequency in the system. The proposed strategy has been validated through the MATLAB/Simulink simulation tool, making a comparison with the classic MPC control with variable switching frequency.

II. SYSTEM DESCRIPTION

This system [Fig. 1] consists of a three-phase STATCOM four-wire based on two-level H-bridge (CHB) converters. Each CHB line is connected with independent DC-links for each phase and the neutral point, using the SiC-MOSFET switching devices. The activation signals are used to control the switching state of each CHB and they are represented as follows, S_{fy} are used to control each cell, with f being the

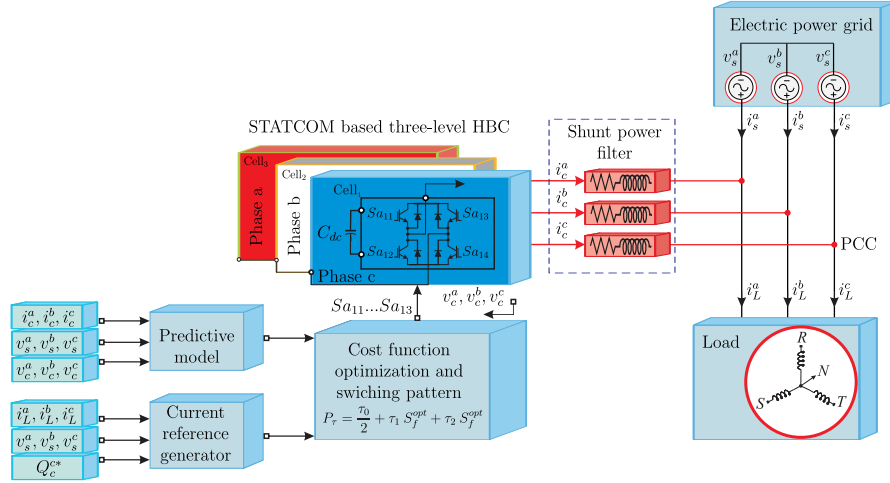


Fig. 1. Control scheme of the proposed modulated MPC.

phase ($f = a, b, c$ and n) and y the switching device in each cell ($y = 1, 2, 3$ or 4). Table I presents the possible combinations of each CHB and the corresponding voltage outputs.

Then, the dynamics of the system's model can be obtained by using Kirchhoff's circuit laws. The imbalance in the three-phase voltage sources, as well as the capacitance and dc-link voltages, are beyond the scope of this paper, and only balanced conditions are considered. Notice that the CHB converter-based STATCOM is connected at the PCC. Next, by applying Kirchhoff's laws for the AC side of the STATCOM, the following equations are obtained:

$$\begin{aligned} \frac{di_c^a}{dt} &= a_1 (v_s^a - R_f i_c^a - n_c S_{ay} v_{dc}^a) \\ \frac{di_c^b}{dt} &= a_1 (v_s^b - R_f i_c^b - n_c S_{by} v_{dc}^b) \\ \frac{di_c^c}{dt} &= a_1 (v_s^c - R_f i_c^c - n_c S_{cy} v_{dc}^c) \end{aligned} \quad (1)$$

being $a_1 = 1/L_f$, R_{dc} a resistor connected in parallel to C_{dc} that concentrates the overall losses in the DC side and R_f is the parasitic (series) resistance of the inductor L_f [4].

A. Classic MPC strategy

In classic MPC controllers, the mathematical model is used to predict the future behavior of the system. In this case, the differential equations of the system in the AC side is

represented by the following equations [4]:

$$\begin{aligned} \frac{di_c^a}{dt} &= a_1 (v_s^a - v_c^a - R_f i_c^a) \\ \frac{di_c^b}{dt} &= a_1 (v_s^b - v_c^b - R_f i_c^b) \\ \frac{di_c^c}{dt} &= a_1 (v_s^c - v_c^c - R_f i_c^c). \end{aligned} \quad (2)$$

Then, the MPC can be obtained by using a forward-Euler discretization method due to its simplicity, however other discretization methods can be used such as the matrix factorization introduced by Cayley-Hamilton [22]. The discrete-time model is given by:

$$\begin{aligned} \hat{i}_{c[k+1|k]}^a &= a_2 i_{c[k]}^a + a_3 (v_{s[k]}^a - v_{c[k]}^a) \\ \hat{i}_{c[k+1|k]}^b &= a_2 i_{c[k]}^b + a_3 (v_{s[k]}^b - v_{c[k]}^b) \\ \hat{i}_{c[k+1|k]}^c &= a_2 i_{c[k]}^c + a_3 (v_{s[k]}^c - v_{c[k]}^c) \end{aligned} \quad (3)$$

TABLE I
POSSIBLE COMBINATIONS OF ACTIVATION SIGNALS

Sa_1	Sa_3	Sa_2	Sa_4	v_c^a
1	0	0	1	$+v_{dc}$
1	1	0	0	0
0	0	1	1	0
0	1	1	0	$-v_{dc}$

being $a_2 = \left(1 - \frac{R_f T_s}{L_f}\right)$ and $a_3 = T_s/L_f$.

In the case of a current control, the typical cost function is defined as the difference between reference currents and the predicted currents:

$$\begin{aligned} \lambda_a &= \|i_c^{a*} - \hat{i}_{c[k+1]}^a\|^2 \\ \lambda_b &= \|i_c^{b*} - \hat{i}_{c[k+1]}^b\|^2 \\ \lambda_c &= \|i_c^{c*} - \hat{i}_{c[k+1]}^c\|^2. \end{aligned} \quad (4)$$

Next, the cost function is evaluated for each switching state and for each phase. The switching state that minimizes the cost function is applied to each phase of the CHB STATCOM during the next sampling time causing a variable switching frequency for each phase.

B. Current reference generation

The current references are necessary to evaluate the cost function in (4). For simplicity, the phase currents and voltages are translated to the $\alpha - \beta$ subspace by using Clarke's transformation matrix:

$$\mathbf{T} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}. \quad (5)$$

Then, the current references in $\alpha - \beta$ subspace in function of active and reactive power are:

$$\begin{bmatrix} i_{c\alpha}^* \\ i_{c\beta}^* \end{bmatrix} = \frac{1}{(v_{s\alpha})^2 + (v_{s\beta})^2} \begin{bmatrix} v_{s\alpha} & v_{s\beta} \\ v_{s\beta} & -v_{s\alpha} \end{bmatrix} \begin{bmatrix} P_c^* \\ Q_c^* \end{bmatrix}. \quad (6)$$

In order to have a unity power factor on the grid side $P_c^* = 0$, then the STATCOM does not absorb active power and the instantaneous reactive power reference can be written as the following:

$$Q_c^* = -Q_L = v_{s\alpha} i_{L\beta} - v_{s\beta} i_{L\alpha} \quad (7)$$

where Q_L is compensated by the CHB STATCOM system. The STATCOM phase currents references used in the optimization process are:

$$\begin{bmatrix} i_c^{a*} \\ i_c^{b*} \\ i_c^{c*} \end{bmatrix} = \mathbf{T}^{-1} \begin{bmatrix} i_{c\alpha}^* \\ i_{c\beta}^* \\ i_{c0}^* \end{bmatrix}. \quad (8)$$

III. PROPOSED MODULATED MPC STRATEGY

The proposed modulation strategy uses the SVM as shown in the [Fig. 2]. The two adherent stress vectors V_1 and V_2 , called sector, are used, of which there are 12 sectors in total. Then two current predictions are made and two cost functions λ_1 and λ_2 are obtained, the null vector V_0 is calculated separately for each phase and adding the functions of null costs per phase. Once the optimal vector is evaluated, the duty cycles for λ_1 and λ_2 are calculated and then, the estimated

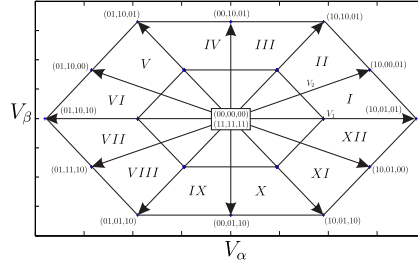


Fig. 2. Three-level H-bridge STATCOM space vector diagram.

duty cycles of every switch is applied. The calculation of the cost function is evaluated with the following function:

$$\begin{aligned} \tau_0 &= K/\sqrt{\lambda_0} \\ \tau_1 &= K/\sqrt{\lambda_1} \\ \tau_2 &= K/\sqrt{\lambda_2} \end{aligned} \quad (9)$$

$$\tau_0 + \tau_1 + \tau_2 = T_s. \quad (10)$$

By solving the system of (9), it is possible to obtain the expression for K and the expressions for the duty cycles τ_0 , τ_1 and τ_2 for each vector, that are given as:

$$\tau_1 = \frac{\sqrt{\lambda_0}\sqrt{\lambda_2}}{\sqrt{\lambda_0}\sqrt{\lambda_1} + \sqrt{\lambda_0}\sqrt{\lambda_2} + \sqrt{\lambda_1}\sqrt{\lambda_2}} \quad (11)$$

$$\tau_2 = \frac{\sqrt{\lambda_0}\sqrt{\lambda_1}}{\sqrt{\lambda_0}\sqrt{\lambda_1} + \sqrt{\lambda_0}\sqrt{\lambda_2} + \sqrt{\lambda_1}\sqrt{\lambda_2}} \quad (12)$$

$$\tau_0 = 1 - \tau_1 - \tau_2 \quad (13)$$

Then, according to these expressions, the new cost function, which is evaluated at every sampling time for each phase, is defined as:

$$\lambda = \tau_1 \sqrt{\lambda_1} + \tau_2 \sqrt{\lambda_2}. \quad (14)$$

Finally, the optimization algorithm selects the optimal vector S_f^{opt} for each firing signals of each cell by the evaluation and minimization of the predefined cost function represented by (14), to apply a switching equation which represents the duty cycle of each transistor in the following equation:

$$P_r = \frac{\tau_0}{2} + \tau_1 S_f^{opt} + \tau_2 S_f^{opt}. \quad (15)$$

IV. THEORETICAL ANALYSIS

This section shows the theoretical results of the proposed MPC modulation using the MATLAB/Simulink simulation tool. A numerical integration based on ode1 Euler using a fixed step of $1\mu s$ and sampling time of $T_s = 50\mu s$ is selected. The grid frequency and peak voltage are set 50 Hz and 310.2 V, respectively. Other electrical parameters are $v_{dc} = 380$ V, $R_f = 0.3\Omega$, $L_f = 10$ mH, $R_L = 23.2\Omega$ and $L_L = 55$ mH.

Initially the system is balanced and with reactive power, then the two-level CHB STATCOM is connected to the $t = 0.04$ s, compensating the reactive power of the grid showing a fast dynamic response for the active power with an overshoot of 32 % and a settling time of approximately 1 ms. The dynamic response for classic MPC is quantified with an overshoot of 21.5 % and a settling time of approximately 1 ms. In this test the active and reactive power in the grid are set to $Q_s = 3\,000$ VAR and $P_s = 4\,000$ W, respectively as shown in Fig. 3 and Fig. 4 for the modulated MPC and the classic MPC respectively. The power RMS ripple of the system can be estimated through the next equation:

$$\text{RMS(ripple)} = \sqrt{\text{RMS}(\text{power})^2 - \text{Mean}(\text{power})^2} \quad (16)$$

where the active and reactive power ripple are 112 W and 96 VAR respectively for the modulated MPC. As for classic MPC, the active and reactive power ripples are 112 W and 150 VAR respectively.

On the other hand, Fig. 5 (above) shows the monitoring of the measured current and the reference current in phase a , and

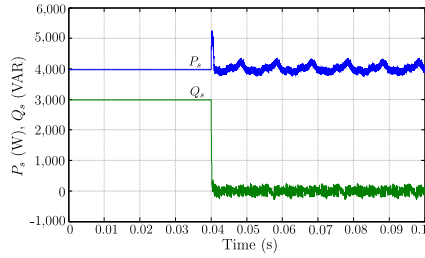


Fig. 3. Three-level H-bridge STATCOM transient response, active and reactive power compensation in the grid using Modulated MPC.

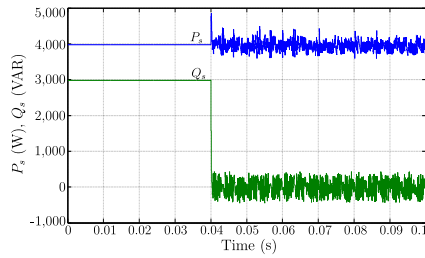


Fig. 4. Three-level H-bridge STATCOM transient response, active and reactive power compensation in the grid using classic MPC.

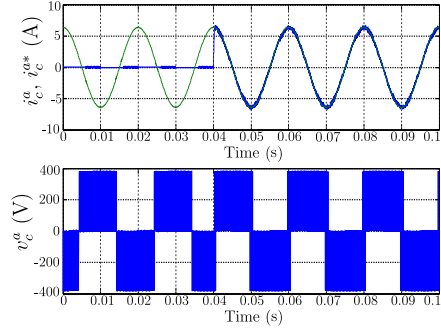


Fig. 5. Transient response of the measurement of the measured current and the reference current (above), output voltage of the H-bridge converter (bottom).

below it shows H-Bridge converter output voltage, showing three levels of voltage (v_{dc} , $-v_{dc}$ and 0). The capacity of current tracking of the proposed controller can be quantifiable by means of the following formula:

$$\text{MSE}(i_{s\gamma}) = \sqrt{\frac{1}{N} \sum_{k=1}^N (i_{s\gamma}(k) - i_{s\gamma}^*(k))^2} \quad (17)$$

where the MSE of the a phase current are, for the modulated and classic MPC, approximately 0.2035 and 0.3037 A respectively. Then, a comparison between the proposed controller and the classic MPC controller is performed. Fig. 6 summarizes the comparison where it can be seen a greater current ripple as well as a widespread harmonic spectrum of the classic MPC. The harmonic spectrum shows a high amplitude for the switching frequency and their corresponding multiples, validating the fixed switching frequency for the proposed controller. By using the THD as a parameter of performance represented by the following equation:

$$\text{THD}(i) = \sqrt{\frac{1}{i_1^2} \sum_{j=2}^N (i_j)^2} \quad (18)$$

where i_1 is the fundamental current and i_j are the harmonic currents. The proposed controller shows an improvement of the THD due to it decreases from 5.04% (classic MPC) to 2.94% (proposed controller).

V. CONCLUSION

In this paper, an MPC is used in conjunction with SVM strategy to provide a constant switching frequency of the current controller of a two-level three-phase four wire CHB STATCOM. As observed from the results, the proposed controller provides a fast dynamic response and easy inclusion of constraints as classic MPC. The proposed controller also provides a reduction of the current ripples as well as a

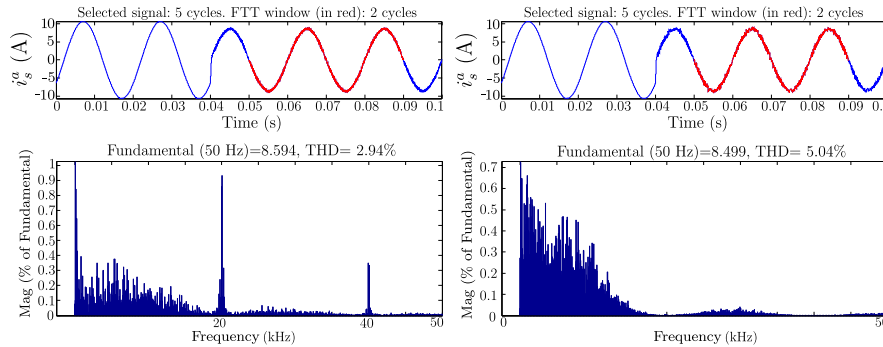


Fig. 6. Comparative analysis of the THD of the electric network current comparing the proposed MPC (left) and the classic MPC (right).

reduction of the THD (around 40 % of the classic MPC), reactive power compensation with less power ripple and taking into account increasing the dc bus voltage from 343 V (classic MPC) to 380 V (modulated MPC).

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Analysis of H-Bridge STATCOM with Fault Phase Controlled by Modulated Predictive Current Control

Alfredo Renault, Magno Ayala, Julio Pacher, Leonardo Comparatore, Raul Gregor and Marco Rivera

Abstract—This paper presents the model-based predictive current control (MPC) applied to a four-wire three-phase STATCOM based on the three-level H-Bridge converter. The main advantages of MPC are its simplicity, easy inclusion of restrictions and fast dynamic response. However, MPC uses a variable switching frequency and this causes a lot of current ripple and a high total harmonic distortion (THD). This article proposes a modulation strategy, at a fixed switching frequency, in order to mitigate the propagation of the THD of the current injected in the point of common coupling (PCC). It is considered a critical operation of the STATCOM operating with a fault on one of the phases of the electrical network. Theoretical results based on simulations are provided to show the performance of the proposed control.

Keywords—Active power filters, fault phase, H-bridge converter, predictive current control, unbalanced load.

NOMENCLATURE

APF	Active power filter.
CHB	Cascade H-bridge.
FCS-MPC	Finite-control-set model predictive control.
MPC	Model predictive control.
PCC	Point of common coupling.
STATCOM	Static compensator.
SVM	Space vector modulation.
THD	Total harmonic distortion.
C_{dc}	DC-link capacitor.
$\lambda_a, \lambda_b, \lambda_c$	MPC cost functions.
$i_s^a, i_s^b, i_s^c, i_s^n$	Power grid phase currents.
i_L^a, i_L^b, i_L^c	Load phase currents.
i_c^a, i_c^b, i_c^c	STATCOM phase currents.
$\hat{i}_c^a, \hat{i}_c^b, \hat{i}_c^c, \hat{i}_c^n$	STATCOM phase current predictions.
$i_{c\alpha}, i_{c\beta}$	STATCOM currents in the $\alpha - \beta$ subspace.
$i_c^{a*}, i_c^{b*}, i_c^{c*}$	STATCOM phase current references.
v_c^a, v_c^b, v_c^c	STATCOM phase voltages.
n_c	Number of cells.
P_c^*	Instantaneous active power reference.
Q_c^*	Instantaneous reactive power reference.
Q_L	Instantaneous reactive load power.
T	Clarke's transformation matrix.
τ_0, τ_1, τ_2	Vectors duty cycles.
T_s	Sampling time.
V_{dc}	DC-link voltage.

A. Renault, M. Ayala, J. Pacher, L. Comparatore and R. Gregor are with the Laboratory of Power and Control Systems, Faculty of Engineering, Universidad Nacional de Asunción, Paraguay e-mail: arenaul, mayala, jpacher, lcomparatore & rgregor @ing.una.py (see <http://www.dspsc.com.py/>).

Prof. Marco Rivera, Department of Electrical Engineering, Centro Tecnológico de conversión de Energía, Facultad de Ingeniería, Universidad de Talca, Campus Curicó, Chile e-mail: marcoriv@utalca.cl (see <https://marcorivera.cl/>).

I. INTRODUCTION

THE STATCOM are regulation devices based on voltage source power converters (VSC) and have the ability to absorb and deliver energy in the AC power transmission and distribution systems [1], [2]. STATCOMs are used to mitigate oscillations in the transmission line, ability to regulate voltage, improve the system stability, reduce several transients, voltage flicker, sag-swell and to control the active and reactive power of the system [3], which is addressed in this article. One of the most important challenges is to minimize short-term disturbances, especially in unbalanced power grid failures [4]–[6]. In the presence of power supply failures, STATCOM helps the system by injecting reactive current to maintain the bus voltage at the desired value and in situations subsequent to the fault it can also improve the transient stability by damping the oscillations [7], [8].

On the other hand, STATCOM's performance under conditions of load imbalance depends largely on its control strategy [9], [10]. The MPC applied to the control of the power converters has been feasible today due to the advancement of the microprocessors and several advantages are obtained as easy inclusion of non-linearities that make it suitable for multivariable systems [11], as shown in several studies of the MPC control applied to many converters, such as matrix converters [12]–[15], active power filters [16]–[20] and multi-phase motors [21]–[25]. Among the disadvantages of the MPC are that it produces a variable switching frequency which causes a high THD that propagates to the variable to be controlled and causes curling [26], [27]. In that order, this document proposes a modulation strategy applied to the predictive current control strategy applied to the three-phase STATCOM four-wire, in such a way to compensate the reactive power, reduce the curling of the current filter and eliminates the neutral current when a phase voltage fault occurs in the electric distribution network on the load side. The MPC modulation strategy has been validated through simulations by comparing with classic MPC without modulation.

II. SYSTEM DESCRIPTION

This system [Fig. 1] consists of a three-phase STATCOM four-wire based on two-level H-bridge (CHB) converters. Each CHB line is connected with independent DC-links for each phase and the neutral point, using the SIC-MOSFET switching devices. The activation signals are used to control the switching state of each CHB and they are represented as follows, S_{fy} are used to control each cell, with f being the

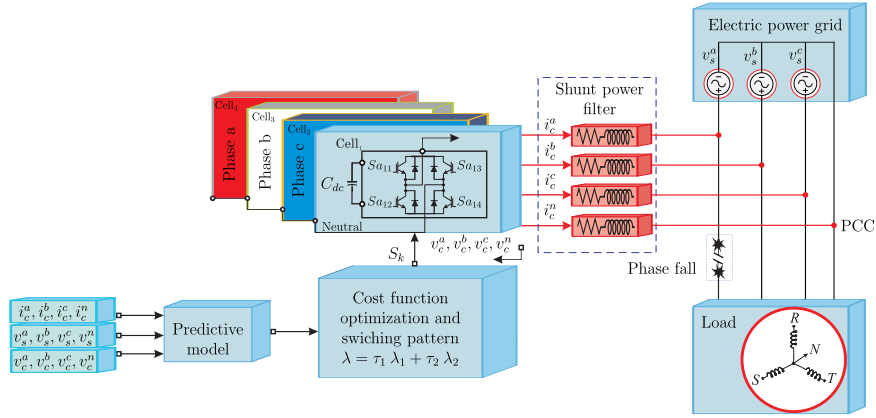


Fig. 1. Control scheme of the proposed modulated MPC.

phase ($f = a, b, c$ and n) and y the switching device in each cell ($y = 1, 2, 3$ or 4). Table I presents the possible combinations of each CHB and the corresponding voltage outputs. Then, the dynamics of the system's model can be obtained by using Kirchhoff's circuit laws. The imbalance in the three-phase voltage sources, as well as the capacitance and dc-link voltages, are beyond the scope of this paper, and only balanced conditions are considered. Notice that the CHB converter-based STATCOM is connected at the PCC. Next, by applying Kirchhoff's laws for the AC side of the STATCOM, the following equations are obtained:

$$\begin{aligned} \frac{di_c^a}{dt} &= a_1 (v_s^a - R_f i_c^a - n_c S a_y v_{dc}^a) \\ \frac{di_c^b}{dt} &= a_1 (v_s^b - R_f i_c^b - n_c S b_y v_{dc}^b) \\ \frac{di_c^c}{dt} &= a_1 (v_s^c - R_f i_c^c - n_c S c_y v_{dc}^c) \\ \frac{di_c^n}{dt} &= a_1 (v_s^n - R_f i_c^n - n_c S c_y v_{dc}^n) \end{aligned} \quad (1)$$

being $a_1 = 1/L_f$, R_{dc} a resistor connected in parallel to C_{dc} that concentrates the overall losses in the DC side and R_f is the parasitic (series) resistance of the inductor L_f [28].

A. Classic MPC strategy

In classic MPC controllers, the mathematical model is used to predict the future behavior of the system. In this case, the differential equations of the system in the AC side is represented by the following equations [28]:

$$\begin{aligned} \frac{di_c^a}{dt} &= a_1 (v_s^a - v_c^a - R_f i_c^a) \\ \frac{di_c^b}{dt} &= a_1 (v_s^b - v_c^b - R_f i_c^b) \\ \frac{di_c^c}{dt} &= a_1 (v_s^c - v_c^c - R_f i_c^c) \\ \frac{di_c^n}{dt} &= a_1 (v_s^n - v_c^n - R_f i_c^n). \end{aligned} \quad (2)$$

Then, the MPC can be obtained by using a forward-Euler discretization method due to its simplicity, however other discretization methods can be used such as the matrix factorization introduced by Cayley-Hamilton [29]. The discrete-time model is given by:

$$\begin{aligned} \hat{i}_{c[k+1|k]}^a &= a_2 \hat{i}_{c[k]}^a + a_3 (v_{s[k]}^a - v_{c[k]}^a) \\ \hat{i}_{c[k+1|k]}^b &= a_2 \hat{i}_{c[k]}^b + a_3 (v_{s[k]}^b - v_{c[k]}^b) \\ \hat{i}_{c[k+1|k]}^c &= a_2 \hat{i}_{c[k]}^c + a_3 (v_{s[k]}^c - v_{c[k]}^c) \\ \hat{i}_{c[k+1|k]}^n &= a_2 \hat{i}_{c[k]}^n + a_3 (v_{s[k]}^n - v_{c[k]}^n) \end{aligned} \quad (3)$$

being $a_2 = (1 - \frac{R_f T_s}{L_f})$ and $a_3 = T_s/L_f$.

In the case of a current control, the typical cost function is defined as the difference between reference currents and the predicted currents:

$$\begin{aligned} \lambda_a &= \| \hat{i}_c^{a*} - \hat{i}_{c[k+1]}^a \|^2 \\ \lambda_b &= \| \hat{i}_c^{b*} - \hat{i}_{c[k+1]}^b \|^2 \\ \lambda_c &= \| \hat{i}_c^{c*} - \hat{i}_{c[k+1]}^c \|^2 \\ \lambda_n &= \| \hat{i}_c^{n*} - \hat{i}_{c[k+1]}^n \|^2. \end{aligned} \quad (4)$$

Next, the cost function is evaluated for each switching state and for each phase. The switching state that minimizes the

TABLE I
POSSIBLE COMBINATIONS OF ACTIVATION SIGNALS

Sa_1	Sa_3	Sa_2	Sa_4	v_c^a
1	0	0	1	$+v_{dc}$
1	1	0	0	0
0	0	1	1	0
0	1	1	0	$-v_{dc}$

cost function is applied to each phase of the CHB STATCOM during the next sampling time causing a variable switching frequency for each phase.

B. Current reference generation

The current references are necessary to evaluate the cost function in (4). For simplicity, the phase currents and voltages are translated to the $\alpha - \beta$ subspace by using Clarke's transformation matrix:

$$\mathbf{T} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}. \quad (5)$$

Then, the current references in $\alpha - \beta$ subspace in function of active and reactive power are:

$$\begin{bmatrix} i_{c\alpha}^* \\ i_{c\beta}^* \end{bmatrix} = \frac{1}{(v_{s\alpha})^2 + (v_{s\beta})^2} \begin{bmatrix} v_{s\alpha} & v_{s\beta} \\ v_{s\beta} & -v_{s\alpha} \end{bmatrix} \begin{bmatrix} P_c^* \\ Q_c^* \end{bmatrix}. \quad (6)$$

and i_{c0}^* simplified is:

$$i_{c0}^* = i_{L0} \quad (7)$$

In order to have a unity power factor on the grid side $P_c^* = 0$, then the STATCOM does not absorb active power and the instantaneous reactive power reference can be written as:

$$Q_c^* = -Q_L = v_{s\alpha} i_{L\beta} - v_{s\beta} i_{L\alpha} \quad (8)$$

where Q_L is compensated by the CHB STATCOM system. The STATCOM phase currents references used in the optimization process are:

$$\begin{bmatrix} i_{c\alpha}^{a*} \\ i_{c\alpha}^{b*} \\ i_{c\alpha}^{c*} \end{bmatrix} = \mathbf{T}^{-1} \begin{bmatrix} i_{c\alpha}^* \\ i_{c\beta}^* \\ i_{c0}^* \end{bmatrix}. \quad (9)$$

III. PROPOSED MODULATED MPC STRATEGY

The general scheme of the proposed modulated MPC is shown in [Fig. 1]. This predictive control strategy uses two active vectors in conjunction with a switching pattern [Fig. 2], therefore it can be seen as space vector modulation (SVM). This method first follows the same procedure as the classic MPC strategy explained in the previous section. After the evaluation of the current predictions (3), currents references (9) and cost function (4), the optimal voltage vector is located in the sector given by the two active vector nearest to the optimum switching state. Then, the proposed method evaluates the cost function, namely λ_1 and λ_2 , of each active voltage

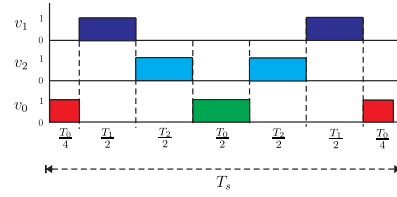


Fig. 2. Switching pattern of the proposed modulated MPC.

vectors. Next, the duty cycles are computed by solving the following equation:

$$\begin{aligned} \tau_0 &= K/\lambda_0 \\ \tau_1 &= K/\lambda_1 \\ \tau_2 &= K/\lambda_2 \end{aligned} \quad (10)$$

$$\tau_0 + \tau_1 + \tau_2 = T_s. \quad (11)$$

By solving the system of (10), it is possible to obtain the expression for K and the expressions for the duty cycles for each vector, that are given as:

$$\tau_1 = \frac{\lambda_0 \lambda_2}{\lambda_0 \lambda_1 + \lambda_0 \lambda_2 + \lambda_1 \lambda_2} \quad (12)$$

$$\tau_2 = \frac{\lambda_0 \lambda_1}{\lambda_0 \lambda_1 + \lambda_0 \lambda_2 + \lambda_1 \lambda_2} \quad (13)$$

$$\tau_0 = 1 - \tau_1 - \tau_2 \quad (14)$$

Then, according to these expressions, the new cost function, which is evaluated at every sampling time for each phase, is defined as:

$$\lambda = \tau_1 \lambda_1 + \tau_2 \lambda_2. \quad (15)$$

Finally, the algorithm selects the optimal vector S_{fpt}^{opt} for each firing signals of each cell by the evaluation and minimization of the predefined cost function represented by (15).

IV. THEORETICAL ANALYSIS

This section shows the theoretical results of the proposed MPC modulation using the MATLAB/Simulink simulation tool. A numerical integration based on ode1 Euler using a fixed step of $1\mu s$ and sampling time of $T_s = 50\mu s$ is selected. The grid frequency and peak voltage are set 50 Hz and 310.2 V, respectively. Other electrical parameters are $v_{dc} = 500$ V, $R_f = 0.3\Omega$, $L_f = 10$ mH, $R_L = 23.2\Omega$ and $L_L = 55$ mH.

Initially the system is balanced, then the load imbalance occurs due to lack of phase at $t = 0.05$ s, then the two-level CHB STATCOM is connected to the $t = 0.1$ s, compensating the reactive power of the grid showing a fast dynamic response. In this test the active and reactive power in the grid are set to $Q_s = 3000$ VAR and $P_s = 4000$ W, respectively as shown in Fig. 3 (upper) using the classic MPC and modulated MPC (bottom). The large oscillations of the active and reactive power are produced by the load imbalance, in this case, due to

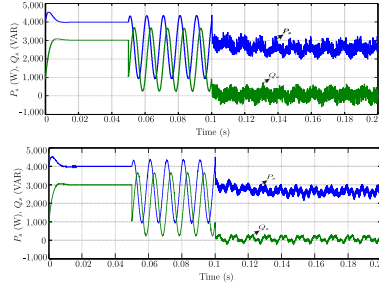


Fig. 3. Two-level H-bridge STATCOM transient response, active and reactive power compensation in the grid using classic MPC (above) and Modulated MPC (bottom).

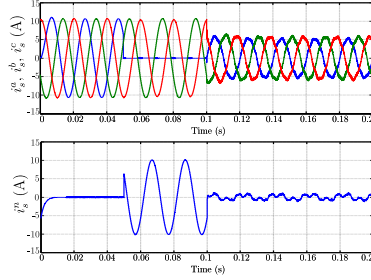


Fig. 4. Transient response of the main phase currents (above) and neutral current compensation (bottom).

lack of phase, which is the greatest imbalance that can occur in the system, when the two-level CHB STATCOM is connected, the proposed control manages to balance and compensate the active and reactive power respectively. It can be appreciated that power ripple (active and reactive) is greatly reduced by the proposed controller in comparison to classic MPC. On the other hand, Fig. 5 (above) shows the monitoring of the measured current and the reference current in phase a , and below it shows H-Bridge converter output voltage. Then, Fig. 4 presents the phase currents a, b, c of the electric grid, it can be seen that when the STATCOM is connected it balances the currents, at the same time, it shows below the compensation of the neutral current. Finally the current injected by the CHB STATCOM presents an excellent and fast-tracking of its reference as shown Fig. 4, for phase a . Similar results have been obtained for phases b and c and have not been included for the sake of conciseness. Then, a comparison between the proposed controller and the classic MPC controller is performed. Fig. 6 summarizes the comparison where it can be seen a greater current ripple as well as a widespread harmonic spectrum of the classic MPC. By using the THD as a parameter of performance represented by the following equation:

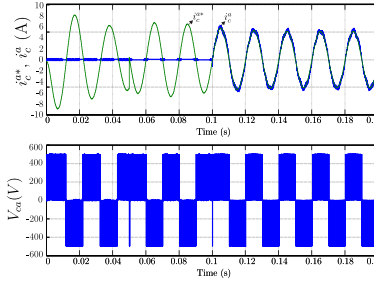


Fig. 5. Transient response of the measurement of the measured current and the reference current (above), output voltage of the H-bridge converter (bottom).

$$THD(i) = \sqrt{\frac{1}{i_1^2} \sum_{j=2}^N (i_j)^2} \quad (16)$$

where i_1 is the fundamental current and i_j are the harmonic currents. The proposed controller shows an improvement of the THD due to it decreases from 10.5% (classic MPC) to 6.53% (proposed controller).

V. CONCLUSION

In this paper, MPC is used in conjunction with SVM strategy to provide a constant switching frequency of the current controller of a two-level three-phase four wire CHB STATCOM. As observed from the results, the proposed controller provides a fast dynamic response and easy inclusion of constraints as classic MPC. The proposed controller also provides a reduction of the current ripples as well as a reduction of the THD (around 4 %), reactive power compensation with less power ripple, neutral current compensation and good balancing of phase currents in the power grid, compared to classic MPC.

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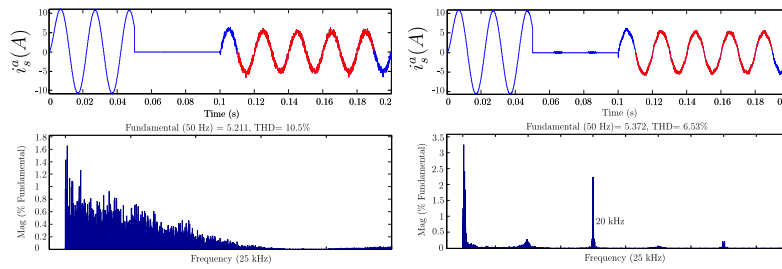


Fig. 6. Comparative analysis of the THD of the electric network current comparing the classic MPC control (left) and the modulated MPC (right).

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Comparative Study of Predictive-Fixed Switching Techniques for a Cascaded H-Bridge Two level STATCOM

Alfredo Renault¹, Magno Ayala¹, Leonardo Comparatore¹, Julio Pachter¹ and Raul Gregor¹

¹Laboratory of Power and Control Systems, Facultad de Ingeniería, Universidad Nacional de Asunción, Paraguay

E-mail: {arenault, mayala, lcomparatore, jpachter & rgregor }@ing.una.py

Abstract—Finite state model predictive control methods are distinguished by a variable switching frequency which causes large current ripples at low sampling frequency. This paper presents a comparative study of two enhanced predictive current control techniques with fixed switching frequency applied to the three-wire cascaded H-bridge two level converter for active power filter applications. Simulation results are developed to demonstrate the performance of the two proposed predictive control techniques in terms of mean square error, root mean square and total harmonic distortion as figures of merit, thus concluding the advantages and limitations of each technique at transient and steady states.

Index Terms—Active power filter, cascaded H-bridge power converter, finite state model predictive control, fixed switching frequency.

NOMENCLATURE

APF	Active power filter.
CHB	Cascade H-bridge.
FCS-MPC	Finite-control-set model predictive control.
MPC	Model predictive control.
MSE	Mean square error.
PCC	Point of common coupling.
RMS	Root mean square.
STATCOM	Static compensator.
THD	Total harmonic distortion.
VSI	Voltage source inverter.
C_{dc}	DC-link capacitor.
g_a, g_b, g_c	FCS-MPC cost functions.
i_s^a, i_s^b, i_s^c	Power grid phase currents.
i_L^a, i_L^b, i_L^c	Load phase currents.
i_c^a, i_c^b, i_c^c	STATCOM phase currents.
$\hat{i}_c^a, \hat{i}_c^b, \hat{i}_c^c$	STATCOM phase current predictions.
$i_{c\alpha}, i_{c\beta}$	STATCOM currents in the $\alpha - \beta$ subspace.
$i_c^{a*}, i_c^{b*}, i_c^{c*}$	STATCOM phase current references.
v_c^a, v_c^b, v_c^c	STATCOM phase voltages.
n_c	Number of cells.
P_c^*	Instantaneous active power reference.
P_L	Instantaneous active load power.
Q_c^*	Instantaneous reactive power reference.
Q_L	Instantaneous reactive load power.
T	Clarke's transformation matrix.
T_s	Sampling time.
V_{dc}	DC-link voltage.

I. INTRODUCTION

Due to the increase of non-linear and reactive loads in recent years, there was an increase of the harmonics amplitudes in the electrical distribution network and the consumption of reactive power [1]. To mitigate this problem, one of the main current solutions to this problem is the use of APF which is responsible for compensating the harmonics of the electrical network and reactive power [2]. APFs are based on power converters such as VSI [3], NPC [4] and H-Bridges [5], [6]. APFs based on H-bridge converters with SiC-MOSFET switching devices have several advantages, such as the possibility of scalability, modular structure and higher switching frequency [7]. Due to these advantages, they have been object of study and are now considered a very competitive topology in the new generation APF based on power converters and can be applied to the electrical distribution power grid [8]. On the other hand, nowadays, MPC is considered a valid alternative to classic controllers and is very used in different applications, due to the improvement of the micro-processor technology, which allows a higher computation speed where the MPC control offers several advantages such as speed response and easy inclusion of no linearities, which makes it suitable for multivariable systems [9]. There are several studies of the MPC control applied to power converters and complex systems such as PFs [10], [11], multiphase machines [12]–[15], matrix converters [16], [17], among others. However, some of the main disadvantages presented by MPC control are stability, steady state error and variable switching frequency which causes high peaks current ripple in the converter output and power losses [18]–[21].

This paper proposes a comparative study of modulated MPC control methods applied to the three-phase APF based on two-level H-bridge converters, obtaining a fixed switching frequency. The comparison is made in terms of MSE current tracking, power ripple RMS and the grid current THD as figures of merit. This paper is organized as follows: Section II describes the three-phase H-bridge APF topology. Section III and Section IV expose the modulated MPC strategies to compare. Section V illustrates the performance of the proposed techniques considering the simulation results. Finally, the conclusion is presented in Section VI.

II. SYSTEM DESCRIPTION

The system under study consists in a two-level three-phase CHB STATCOM depicts in Fig. 1. Notice that each cell of the CHB have an independent DC-link and four switching devices, typically IGBTs or SiC MOSFETs. Then, four firing signals, represented by S_{fxy} are used to control each cell, being f the phase ($f = a, b$ or c), x the cell number in each phase and y the switching device in each cell ($y = 1, 2, 3$ or 4). Table I shows the allowed combination of the firing signal taking phase “a” as example. Similar analysis can be easily extended to other phases considering allowed combinations and avoid short circuit in the DC-link of each cell.

Then, the dynamic of the system’s model can be obtained by using Kirchhoff’s circuit laws. The imbalance in the three-phase voltage sources as well as the capacitance and DC-link voltages are beyond the scope of this paper, and only balance conditions are considered. Notice that the CHB converter-based STATCOM is connected at the PCC. Next, by applying Kirchhoff’s laws for the ac side of the STATCOM, the following equations are obtained:

$$\begin{aligned} \frac{di_c^a}{dt} &= 1/L_f (v_s^a - R_f i_c^a - n_c S a_{ij} v_{dc}^a) \\ \frac{di_c^b}{dt} &= 1/L_f (v_s^b - R_f i_c^b - n_c S b_{ij} v_{dc}^b) \\ \frac{di_c^c}{dt} &= 1/L_f (v_s^c - R_f i_c^c - n_c S c_{ij} v_{dc}^c) \end{aligned} \quad (1)$$

$$\begin{aligned} \frac{dv_{dc}^a}{dt} &= \frac{S a_{ij} i_c^a}{C_{dc}} - \frac{v_{dc}^a}{R_{dc} C_{dc}} \\ \frac{dv_{dc}^b}{dt} &= \frac{S b_{ij} i_c^b}{C_{dc}} - \frac{v_{dc}^b}{R_{dc} C_{dc}} \\ \frac{dv_{dc}^c}{dt} &= \frac{S c_{ij} i_c^c}{C_{dc}} - \frac{v_{dc}^c}{R_{dc} C_{dc}} \end{aligned} \quad (2)$$

being, R_{dc} a resistor connected in parallel to C_{dc} that concentrates the overall losses in the DC side and R_f is the parasitic (series) resistance of the inductor L_f .

A. Classic FCS-MPC strategy

In classic FCS-MPCs the mathematical model is used to predict the future behavior of the system. In this case, the differential equations of the system in the AC side is represented by the following equations:

$$\begin{aligned} \frac{di_c^a}{dt} &= 1/L_f (v_s^a - v_c^a - R_f i_c^a) \\ \frac{di_c^b}{dt} &= 1/L_f (v_s^b - v_c^b - R_f i_c^b) \\ \frac{di_c^c}{dt} &= 1/L_f (v_s^c - v_c^c - R_f i_c^c). \end{aligned} \quad (3)$$

Then, the predictive model can be obtained by using a forward-Euler discretization method due to its simplicity, however other discretization methods can be used such as

TABLE I
POSSIBLE COMBINATIONS OF ACTIVATION SIGNALS

$S a_{11}$	$S a_{13}$	$S a_{12}$	$S a_{14}$	v_{dc}^a
1	0	0	1	$+v_{dc}$
1	1	0	0	0
0	0	1	1	0
0	1	1	0	$-v_{dc}$

the matrix factorization introduced by Cayley-Hamilton. The discrete-time model is given by:

$$\begin{aligned} \hat{i}_{c[k+1|k]}^a &= A_1 i_{c[k]}^b + T_s/L_f (v_{s[k]}^a - v_{c[k]}^a) \\ \hat{i}_{c[k+1|k]}^b &= A_1 i_{c[k]}^b + T_s/L_f (v_{s[k]}^b - v_{c[k]}^b) \\ \hat{i}_{c[k+1|k]}^c &= A_1 i_{c[k]}^c + T_s/L_f (v_{s[k]}^c - v_{c[k]}^c) \end{aligned} \quad (4)$$

being $A_1 = \left(1 - \frac{R_f T_s}{L_f}\right)$.

In the case of a current control, the typical cost function is defined as the difference between reference currents and the predicted currents:

$$\begin{aligned} g_a &= \| i_c^{a*} - \hat{i}_{c[k+1]}^a \|^2 \\ g_b &= \| i_c^{b*} - \hat{i}_{c[k+1]}^b \|^2 \\ g_c &= \| i_c^{c*} - \hat{i}_{c[k+1]}^c \|^2. \end{aligned} \quad (5)$$

Next, the cost function is evaluated for each switching states and for each phase. The switching state that minimizes the cost function is applied to each phase of the CHB STATCOM during the next sampling time causing a variable switching frequency for each phase.

B. Current reference generation

For the evaluation of the cost function in (5) is necessary the current references. For simplicity, the phase currents and voltages are translated to the $\alpha - \beta$ subspace by using Clarke’s transformation matrix:

$$\mathbf{T} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}. \quad (6)$$

Then, the current references in $\alpha - \beta$ subspace in function of active and reactive power are:

$$\begin{bmatrix} i_{c\alpha}^* \\ i_{c\beta}^* \end{bmatrix} = \frac{1}{(v_{s\alpha})^2 + (v_{s\beta})^2} \begin{bmatrix} v_{s\alpha} & v_{s\beta} \\ v_{s\beta} & -v_{s\alpha} \end{bmatrix} \begin{bmatrix} P_c^* \\ Q_c^* \end{bmatrix}. \quad (7)$$

In order to have a unit power factor on the grid side $P_c^* = 0$, then the STATCOM does not absorb active power and the instantaneous reactive power reference can be written as:

$$Q_c^* = -Q_L = v_{s\alpha} i_{L\beta} - v_{s\beta} i_{L\alpha} \quad (8)$$

where Q_L is compensated by the CHB STATCOM system. The STATCOM phase currents references used in the optimization process are:

$$\begin{bmatrix} i_c^{a*} \\ i_c^{b*} \\ i_c^{c*} \end{bmatrix} = \mathbf{T}^{-1} \begin{bmatrix} i_{c\alpha}^* \\ i_{c\beta}^* \\ 0 \end{bmatrix}. \quad (9)$$

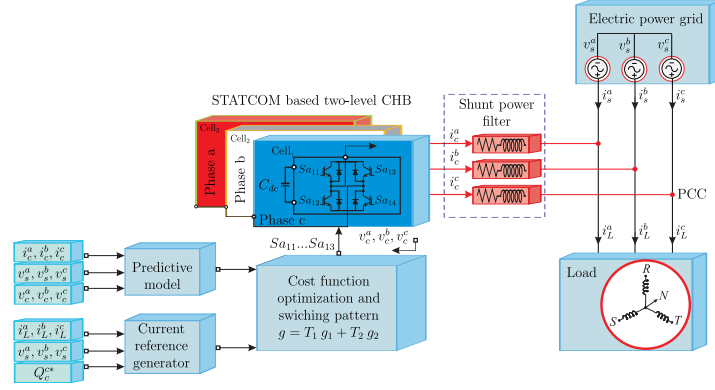


Fig. 1. Control scheme of the proposed modulated FCS-MPC.

III. MODULATED FCS-MPC METHOD (M2PC)

The general scheme of the proposed modulated FCS-MPC is shown in Fig. 1. This M2PC uses two active vectors and two null vectors in conjunction with a switching pattern exposed in Fig. 2, therefore it can be seen as space vector modulation. This method first follows the same procedure as classic FCS-MPC technique explained in the previous section. After the evaluation of the current predictions (4), cost function (5) and currents references (9), the optimum voltage vector is obtained through the combination of the two active vectors and the two null vectors [22], [23]. Then, the proposed method evaluates the cost function, namely g_0 , g_1 and g_2 , of each voltage vector (active and null) to estimate the duty cycles for each vector and these are computed by solving the following equations:

$$T_0 = \frac{K}{g_0} \quad (10)$$

$$T_1 = \frac{K}{g_1} \quad (11)$$

$$T_2 = \frac{K}{g_2} \quad (12)$$

$$T_0 + T_1 + T_2 = T_s \quad (13)$$

By solving the system of (13), it is possible to obtain the expression for K and the expressions for the duty cycles:

$$T_1 = \frac{g_0 g_2}{g_0 g_1 + g_0 g_2 + g_1 g_2} \quad (14)$$

$$T_2 = \frac{g_0 g_1}{g_0 g_1 + g_0 g_2 + g_1 g_2} \quad (15)$$

$$T_0 = 1 - T_1 - T_2 \quad (16)$$

According to these expressions, the new cost function, which is evaluated at every sampling time for each phase, is defined:

$$g = T_1 g_1 + T_2 g_2 \quad (17)$$

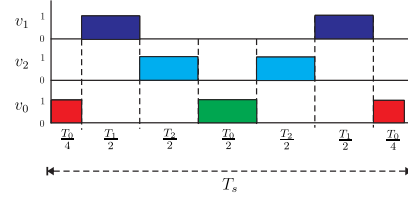


Fig. 2. Switching pattern of the proposed modulated FCS-MPC.

IV. MODULATED FCS-MPC TECHNIQUE (PWM)

The FCS-MPC technique selects an optimal vector from the minimization of the cost function in (5). Instead of applying the chosen voltage vector to the CHB during the whole switching period, which is the procedure in conventional FCS-MPC schemes, then a PWM method is added to the FCS-MPC output to obtain a fixed-switching frequency. The duty cycles depend on the generated voltage level in the CHB where, according to Table I, there are three voltage levels ($+v_{dc}$, $-v_{dc}$ and 0). By using conditions it is possible to estimate the duty cycle for a switching device which obtains a similar voltage level as shown in Table II. The duty cycles generate a fixed switching frequency for every switching device improving the performance over classic FCS-MPC.

TABLE II
POSSIBLE DUTY CYCLES OF ACTIVATION SIGNALS

S_{a11}	S_{a13}	v_c^a
0.95	0.05	$+v_{dc}$
0.5	0.5	0
0.05	0.95	$-v_{dc}$

V. SIMULATION RESULTS

This section exposes the performance of the proposed modulated FCS-MPC techniques by using a MATLAB/Simulink simulation tool. A numerical integration based on Ode1 Euler was used for the calculation of fixed step in the time domain with a relative tolerance of $1 \mu s$ and with $T_s = 50 \mu s$. The grid frequency and voltage are set 50 Hz and 310.2 V, respectively. Other electrical parameters are $v_{dc} = 400$ V, $R_f = 0.09 \Omega$, $L_f = 9$ mH, $R_L = 23.2 \Omega$ and $L_L = 55$ mH.

The two-level CHB STATCOM is connected at $t = 0.02$ s, compensating the reactive power of the grid showing a fast dynamic response for both modulation techniques exposed in Fig. 3. In this test the active and reactive power are set to $Q_L = 3000$ VAR and $P_L = 4000$ W, respectively. The mean value of Q_s for M2PC and PWM are 1.978 and 2.853 VAR respectively, compensating a 99.93 and 99.90 % of the load reactive power. On the other hand, the RMS of P_s and Q_s ripple for M2PC are 87.13 W, 59.94 VAR and for PWM are 164.18 W, 175.38 VAR, respectively. At last, by considering the mean value of P_s for both modulation techniques, the power efficiency of the CHB STATCOM is about 99.30 and 98.86 % for M2PC and PWM, respectively.

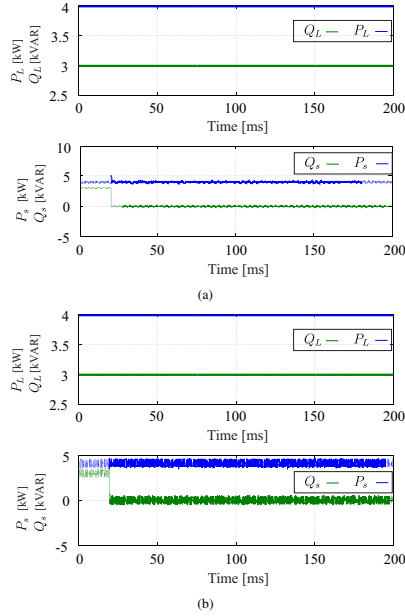


Fig. 3. Two-level CHB STATCOM response for M2PC, active and reactive power compensation, (above) in the load and (bottom) in the power grid: (a) M2PC; (b) PWM.

The current injected by the two-level CHB STATCOM presents an excellent and fast tracking of its reference as shown shown Fig. 4, for phase a . In order to quantify the performance tracking of the injected current, the MSE of the measured current and the reference is considered. The obtained values for both techniques are 166.5 and 373.4 mA for M2PC and PWM, respectively.

Then, Fig. 5 and Fig. 6 show the two-level CHB STATCOM voltage output, which show a two level pattern plus the null voltage level, and the harmonic spectrum for the grid current, where the THD for the grid current are 2.57 and 5.89 % for M2PC and PWM, respectively. It can also be seen in the harmonic spectrum the dominant harmonic switching frequency of 20 kHz and its multiples which is the fixed switching frequency of the system.

Similar results have been obtained for phases b and c and have not been included for the sake of conciseness.

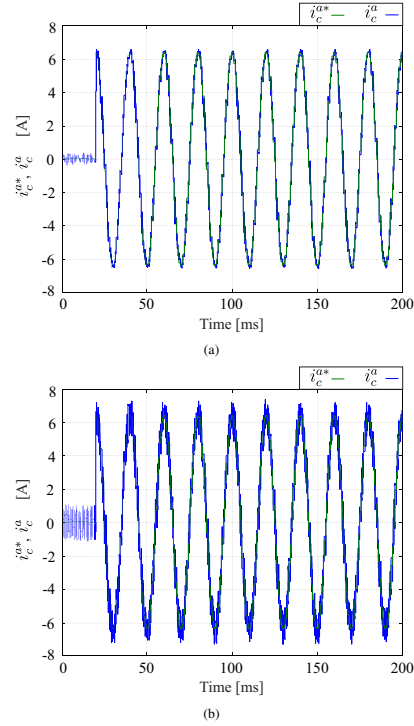


Fig. 4. Two-level CHB STATCOM response for M2PC, active and reactive power compensation, (above) in the load and (bottom) in the power grid: (a) M2PC; (b) PWM.

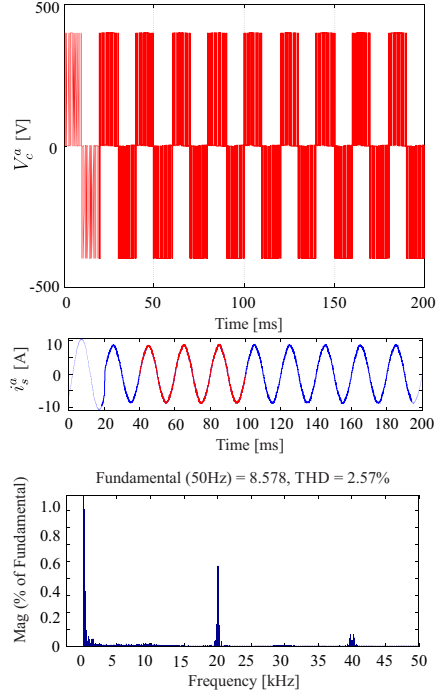


Fig. 5. (above) APF voltage, (middle) the grid current evolution at PCC, (bottom) the THD of the grid current for M2PC.

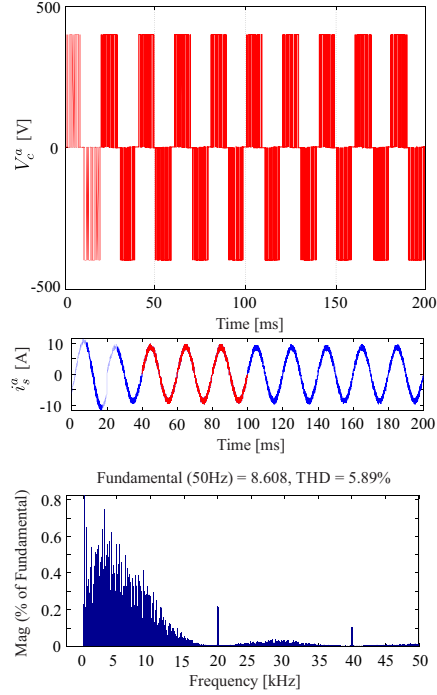


Fig. 6. (above) APF voltage, (middle) the grid current evolution at PCC, (bottom) the THD of the grid current for PWM.

VI. CONCLUSION

This paper has presented a comparative study between two FCS-MPC with fixed switching frequency. It has been shown that both techniques, M2PC and PWM, are powerful alternatives to current controller of a two-level three-phase CHB STATCOM. While, in transient conditions, both techniques have very similar dynamics, in steady states, M2PC techniques shows a better performance over PWM in every considered parameter, such as the current grid THD, the injection current MSE and the RMS power ripple and power efficiency. The only drawback presented for M2PC compared to PWM is the computational cost, which it is assumed to be higher due to the fact that M2PC needs more calculation process to obtain the optimal duty cycles. Still both techniques are considered to be valuable alternatives to classic FCS-MPC with variable switching frequency. From the point of view of the charge of the H-bridge capacitors, further research will be necessary to find an optimal switching pattern.

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Modulated Predictive Current Control Technique for a Three-Phase Four-Wire Active Power Filter based on H-bridge Two-Level Converter

Alfredo Renault, Jorge Rodas, Leonardo Comparatore, Julio Pachter and Raul Gregor

Laboratory of Power and Control Systems, Facultad de Ingeniería, Universidad Nacional de Asunción, Paraguay

E-mail: {arenault, jrodas, lcomparatore, jpachter & rgregor}@ing.una.py

Abstract—Finite-control-set model-based predictive current control (FCS-MPCC) technique is distinguished by a variable switching frequency which causes high harmonic distortion a low sampling frequency. This latter could be considered an undesired behavior for active power filter for grid-connected applications. To overcome this issue, this paper proposes a modulated FCS-MPCC applied to a three-phase four-wire active power filter based on H-bridge converter. Simulation results are developed to demonstrate the efficiency of the proposed modulated FCS-MPCC comparing with classic FCS-MPCC, thus concluding the advantages and limitations of each technique at transient and steady states.

Index Terms—Active power filter, current control, H-bridge converter, model predictive control.

NOMENCLATURE

APF	Active power filter.
CHB	Cascade H-bridge.
FCS-MPCC	Finite-control-set MPCC.
MPCC	Model-based predictive current control.
PCC	Point of common coupling.
STATCOM	Static compensator.
THD	Total harmonic distortion.
C_{dc}	dc-link capacitor.
g_a, g_b, g_c, g_n	FCS-MPCC cost functions.
$i_s^a, i_s^b, i_s^c, i_s^n$	Power grid phase currents.
v_s^a, v_s^b, v_s^c	Power grid phase voltage.
$i_L^a, i_L^b, i_L^c, i_L^n$	Load phase currents.
$i_c^a, i_c^b, i_c^c, i_c^n$	STATCOM phase currents.
$\hat{i}_c^a, \hat{i}_c^b, \hat{i}_c^c, \hat{i}_c^n$	STATCOM phase current predictions.
$i_{c\alpha}, i_{c\beta}, i_{c0}$	STATCOM currents in the $\alpha - \beta - 0$ subspace.
$i_c^{a*}, i_c^{b*}, i_c^{c*}, i_c^{n*}$	STATCOM current references.
v_c^a, v_c^b, v_c^c	STATCOM phase voltages.
n_c	Number of cells.
P_c^*	Instantaneous active power reference.
P_0	Instantaneous active power 0 sequence.
Q_c^*	Instantaneous reactive power reference.
Q_L	Instantaneous reactive load power.
T	Clarke's transformation matrix.

I. INTRODUCTION

APFs based on H-bridge converters equipped with SiC-MOSFETs switching devices have several advantages

such as the possibility of scalability, modular structure and high switching frequency [1], [2]. Due to these advantages, SiC-MOSFETs H-bridge converters have attracted the attention of the research community and currently, they are considered as a real competitive topology in the new generation APF for grid-connected converters [3], [4].

Nowadays, FCS-MPCC is applied with success in complex power electronic applications such as APFs [5], multiphase machines [6], matrix converters [7], among others. The easy inclusion of non-linearities and constraints, as well as its fast dynamic response, makes FCS-MPCC an alternative to classic control methods. Moreover, thanks to the improvement of the microprocessor technology, the implementation of FCS-MPCC algorithm could be performed at higher sampling frequency [8], [9]. However, one of the main disadvantage presented by FCS-MPCC is its variable switching frequency produced by the optimal voltage vectors. This issue may produce current ripple with high peaks in the current to the converter output and power losses [10], [11].

In this context, this article proposes a modulated FCS-MPCC method applied to a four-wire three-phase APF based on two-level H-bridge converters operated at fixed switching frequency through a switching pattern [12], [13]. This allows a better distribution of switching in the power semiconductor devices, thus reducing power losses and the current ripple in the output current of the converter and reducing the THD injected into the electrical power grid [14], [15]. To check the feasibility of the proposal, a comparison is made with the classic FCS-MPCC and the modulated FCS-MPCC, simulation results are presented using the MATLAB/Simulink tool. This paper is organized as follows: Section II describes the three-phase four-wire CHB STATCOM topology. In the same section, the classic FCS-MPC is also introduced. Then, Section III exposes the proposed modulated FCS-MPCC strategy. Section IV illustrates the performance of the proposed techniques considering the simulation results. Finally, the conclusion is presented in Section V.

II. SYSTEM DESCRIPTION

The system under study is a three-phase four-wire APF based on CHB connected in parallel to the electric power grid as shown in Fig. 1. The APF consists of four independent

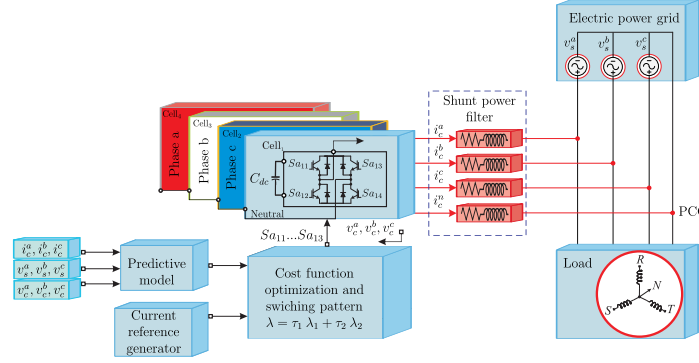


Fig. 1. The control scheme of the proposed modulated FCS-MPCC.

CHB cells with dc-link corresponding to the phases a , b , c and n [16], [17]. Each CHB cell contains four switching devices SiC-MOSFET (which can operate up to 100 kHz) connected in H-bridge S_{fxy} to control each cell, being f the phase ($f = a, b, c$), x cell number in each phase and y the switching device in each cell ($y = 1, 2, 3$ or 4). Table 1 shows the permitted combinations of the activation signals of the switching devices and the voltage vectors at the output of the converter, for the case of phase a , for example. The analysis is similar for the other cells avoiding the short circuit in the dc-link. The dynamics of the system model is obtained using the Kirchhoff circuit laws. The unbalance of the three-phase voltages of the electrical power grid, as well as the capacitance and dc-link voltages, are beyond the scope of this document, and only the equilibrium conditions are considered to obtain the system model. The STATCOM based on the CHB converter is connected to the PCC. Then, applying the laws of Kirchhoff for the ac side of STATCOM, the following equations are obtained:

TABLE I
POSSIBLE COMBINATIONS OF ACTIVATION SIGNALS

S_{a11}	S_{a13}	S_{a12}	S_{a14}	v_c^a
1	0	0	1	$+v_{dc}$
1	1	0	0	0
0	0	1	1	0
0	1	1	0	$-v_{dc}$

$$\begin{aligned}
 \frac{di_c^a}{dt} &= 1/L_f (v_s^a - R_f i_c^a - n_c S_{axy} v_{dc}^a) \\
 \frac{di_c^b}{dt} &= 1/L_f (v_s^b - R_f i_c^b - n_c S_{bxy} v_{dc}^b) \\
 \frac{di_c^c}{dt} &= 1/L_f (v_s^c - R_f i_c^c - n_c S_{cxy} v_{dc}^c) \\
 \frac{di_c^n}{dt} &= 1/L_f (v_s^n - R_f i_c^n - n_c S_{cxy} v_{dc}^n)
 \end{aligned} \quad (1)$$

$$\begin{aligned}
 \frac{dv_{dc}^a}{dt} &= \frac{S_{axy} i_c^a}{C_{dc}} - \frac{v_{dc}^a}{R_{dc} C_{dc}} \\
 \frac{dv_{dc}^b}{dt} &= \frac{S_{bxy} i_c^b}{C_{dc}} - \frac{v_{dc}^b}{R_{dc} C_{dc}} \\
 \frac{dv_{dc}^c}{dt} &= \frac{S_{cxy} i_c^c}{C_{dc}} - \frac{v_{dc}^c}{R_{dc} C_{dc}} \\
 \frac{dv_{dc}^n}{dt} &= \frac{S_{cxy} i_c^n}{C_{dc}} - \frac{v_{dc}^n}{R_{dc} C_{dc}}
 \end{aligned} \quad (2)$$

being R_{dc} a resistor connected in parallel to C_{dc} that concentrates the overall losses in the dc side and R_f, L_f are the resistance and inductor, respectively, that work as a filter at the output of the CHB.

A. Classic FCS-MPCC strategy

Classic FCS-MPCC uses the mathematical model of the system, namely predictive model, to predict its future behavior. In this case, the differential equations of the system in the ac side is represented by the following equations:

$$\begin{aligned}
 \frac{di_c^a}{dt} &= 1/L_f (v_s^a - v_c^a - R_f i_c^a) \\
 \frac{di_c^b}{dt} &= 1/L_f (v_s^b - v_c^b - R_f i_c^b) \\
 \frac{di_c^c}{dt} &= 1/L_f (v_s^c - v_c^c - R_f i_c^c) \\
 \frac{di_c^n}{dt} &= 1/L_f (v_s^n - v_c^n - R_f i_c^n)
 \end{aligned} \quad (3)$$

Then, the predictive model can be obtained by using a forward-Euler discretization method due to its simplicity. However other discretization methods can be used such as

the matrix factorization introduced by Cayley-Hamilton. The discrete-time model is given by [18], [19]:

$$\begin{aligned}\hat{i}_{c[k+1|k]}^a &= A_1 \hat{i}_{c[k]}^b + T_s/L_f \left(v_{s[k]}^a - v_{c[k]}^a \right) \\ \hat{i}_{c[k+1|k]}^b &= A_1 \hat{i}_{c[k]}^c + T_s/L_f \left(v_{s[k]}^b - v_{c[k]}^b \right) \\ \hat{i}_{c[k+1|k]}^c &= A_1 \hat{i}_{c[k]}^n + T_s/L_f \left(v_{s[k]}^c - v_{c[k]}^c \right) \\ \hat{i}_{c[k+1|k]}^n &= A_1 \hat{i}_{c[k]}^n + T_s/L_f \left(v_{s[k]}^n - v_{c[k]}^n \right)\end{aligned}\quad (4)$$

being $A_1 = \left(1 - \frac{R_f T_s}{L_f}\right)$.

In the case of a current control, the typical cost function is defined as the difference between reference currents and the predicted currents [20], [21]:

$$\begin{aligned}g_a &= \| \hat{i}_c^{a*} - \hat{i}_{c[k+1]}^a \|^2 \\ g_b &= \| \hat{i}_c^{b*} - \hat{i}_{c[k+1]}^b \|^2 \\ g_c &= \| \hat{i}_c^{c*} - \hat{i}_{c[k+1]}^c \|^2 \\ g_n &= \| \hat{i}_c^{n*} - \hat{i}_{c[k+1]}^n \|^2.\end{aligned}\quad (5)$$

Next, the cost function is evaluated for each switching states and for each phase. The switching state that minimizes the cost function is applied to each phase of the CHB STATCOM during the next sampling time causing a variable switching frequency for each phase.

B. Current reference generation

For the evaluation of the cost function in (5) is necessary the current references. For simplicity, the phase currents and voltages are translated to the $\alpha - \beta - 0$ subspace by using Clarke's transformation matrix:

$$\mathbf{T} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}. \quad (6)$$

Then, the current references in $\alpha - \beta - 0$ subspace in function of active and reactive power are:

$$\begin{bmatrix} \hat{i}_{c\alpha}^* \\ \hat{i}_{c\beta}^* \end{bmatrix} = \frac{1}{(v_{s\alpha})^2 + (v_{s\beta})^2} \begin{bmatrix} v_{s\alpha} & v_{s\beta} \\ v_{s\beta} & -v_{s\alpha} \end{bmatrix} \begin{bmatrix} P_c^* \\ Q_c^* \end{bmatrix}. \quad (7)$$

and $\hat{i}_{c0}^*$ simplified is:

$$\hat{i}_{c0}^* = i_{L0} \quad (8)$$

Then the STATCOM does compensate the alternate part of the active power and the instantaneous reactive power reference can be written as [22], [23]:

$$P_c^* = -\tilde{P}_L \quad (9)$$

$$Q_c^* = -Q_L = v_{s\alpha} i_{L\beta} - v_{s\beta} i_{L\alpha} \quad (10)$$

$$P_{c0}^* = -P_{L0} = -i_{L0} v_{s0} \quad (11)$$

where Q_L and P_{L0} are compensated by the CHB STATCOM system. The STATCOM phase currents references used in the optimization process are:

$$\begin{bmatrix} \hat{i}_c^{a*} \\ \hat{i}_c^{b*} \\ \hat{i}_c^{c*} \end{bmatrix} = \mathbf{T}^{-1} \begin{bmatrix} \hat{i}_{c\alpha}^* \\ \hat{i}_{c\beta}^* \\ \hat{i}_{c0}^* \end{bmatrix}. \quad (12)$$

III. PROPOSED MODULATED FCS-MPCC STRATEGY

This predictive control strategy uses two active vectors in conjunction with a switching pattern Fig. 2, therefore it can be seen as space vector modulation. This method first follows the same procedure as classic FCS-MPCC strategy explained in the previous section. After the evaluation of the current predictions (4), currents references (12) and cost function (5), the optimum voltage vector is located in sector given by the two active vector nearest to the optimum switching state. Then, the proposed method evaluates the cost function, namely λ_1 and λ_2 , of each active voltage vectors. Next, the duty cycles are computed by solving the following equation:

$$\overbrace{K/\lambda_1}^{\tau_1} + \overbrace{K/\lambda_2}^{\tau_2} = T_s. \quad (13)$$

By solving (13) it is possible to obtain the expression for K and the expressions for the duty cycles for each vector, that are given as:

$$\begin{aligned}\tau_1 &= \frac{\lambda_2}{\lambda_1 + \lambda_2} \\ \tau_2 &= \frac{\lambda_1}{\lambda_1 + \lambda_2}.\end{aligned}\quad (14)$$

Then, according to these expressions, the new cost function, which is evaluated at every sampling time for each phase, is defined as:

$$\lambda = \tau_1 \lambda_1 + \tau_2 \lambda_2. \quad (15)$$

Finally, the optimization algorithm selects the optimum vector S_f^{opt} for each firing signals of each cell by the evaluation and minimization of the predefined cost function represented by (15). To make the thing clearer, Algorithm 1 summarizes the optimization process.

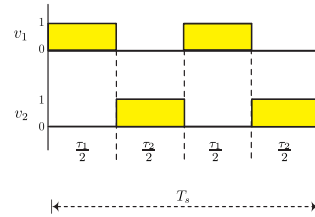


Fig. 2. Switching pattern of the proposed modulated FCS-MPCC.

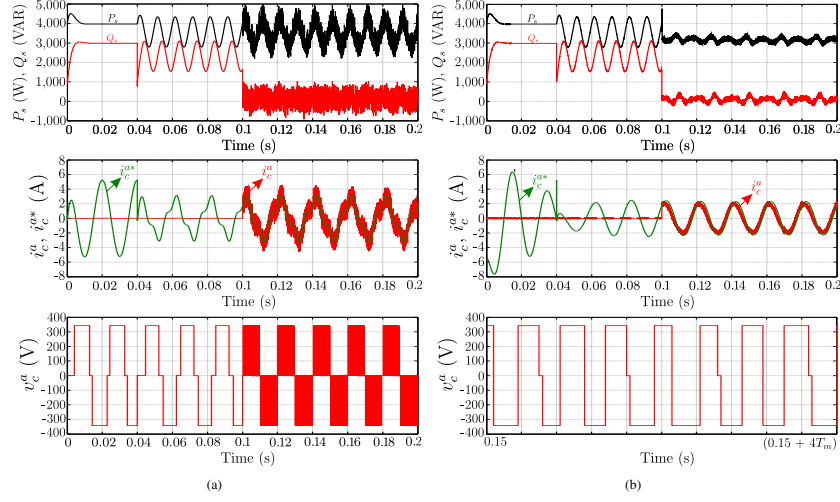


Fig. 4. Comparison of each controller considering: (above) the active power and reactive power compensation, (middle) current of CHB STATCOM and current reference, (bottom) output voltage of CHB STATCOM. (a) Classic FCS-MPCC, (b) Proposed modulated FCS-MPCC.

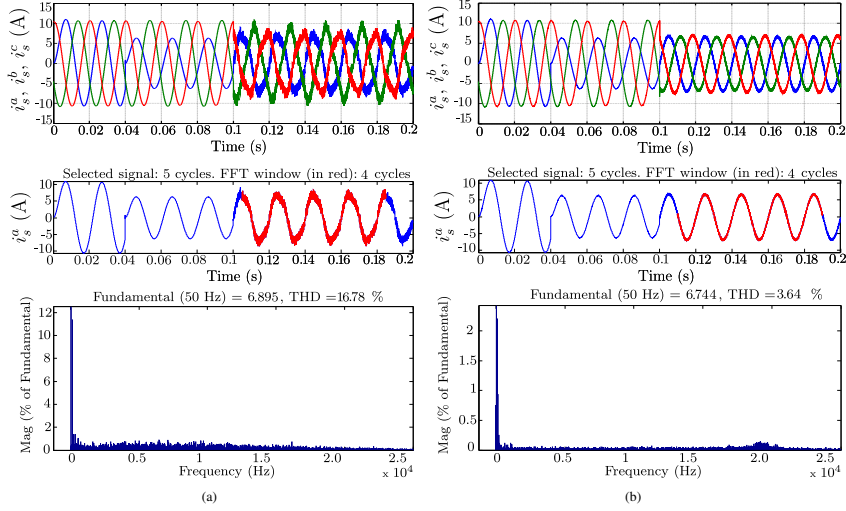


Fig. 5. Comparison of each controller considering: (above) the power grid current evolution, (middle) four sample cycles of power grid current in phase "a" for the calculation of THD, (bottom) the THD of power grid current. (a) Classic FCS-MPCC, (b) Proposed modulated FCS-MPCC.

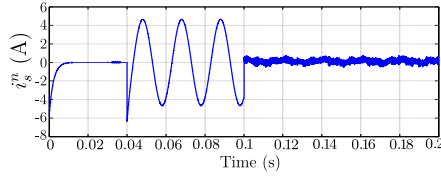


Fig. 6. Neutral current elimination of the modulated FCS-MPCC.

ACKNOWLEDGMENT

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Finite Control Set Model Predictive Control Strategies for a Three-Phase Seven-level Cascade H-Bridge DSTATCOM

Leonardo Comparatore, Alfredo Renault, Julio Pacher, Jorge Rodas and Raúl Gregor

Laboratory of Power and Control Systems
Facultad de Ingeniería, Universidad Nacional de Asunción
Luque, Paraguay
{lcomparatore, arenault, jpacher, jrodas, rgregor}@ing.una.py

Abstract—Despite all advantages of model predictive control, when this control scheme is implemented in power converters, like multilevel cascade H-bridge, it generates a variable switching frequency. This variable switching frequency can deteriorate the performance of the system. This paper examines this problem and proposes two different modulation stages to the model predictive control to solve this issue. A comparative analysis of this modulation stages with conventional predictive control, in terms of total harmonic distortion, reference tracking error, output voltages waveforms, and balance voltages on the capacitors with simulations results to validate the solutions are shown.

Index Terms—Cascade H-bridge converter, fixed switching frequency, predictive control.

I. INTRODUCTION

Novel, complex and sophisticated control approaches for power electronics, are today possible to implement in standard control hardware platforms thanks to the development achieved in digital microprocessors, such digital signal processors (DSPs) and field-programmable gate array (FPGAs) [1]. This has generated a huge advance in the development of distribution static synchronous compensators (DSTATCOMs), because this sophisticated control techniques improve the capability of reducing the problems related to power quality of DSTATCOMs, even with dynamically changing loads [2]. Another major factor in the evolution of DSTATCOM technology are the multilevel converter topologies. The multilevel cascade H-bridge (CHB) converter, in particular, is considered as one of the most suitable configuration for high-power DSTATCOMs [3], this is mainly because the advantages of multilevel CHB converters include low total harmonic distortion, modularity and good scalability, resulting in a better output waveforms quality and, in terms of control strategies, more degrees of freedom [4]. The attention of the research community in control approaches for DSTATCOM and multilevel CHB converters is clearly demonstrated in the technical literature, in [5] was presented a comparison of four different current control techniques. Proportional integral (PI) controllers require the dynamic model of the system in the synchronous reference frame (SRF) also known as dq frame, thus, an extra phase-locked loop (PLL) algorithm and multiple

band-pass filters are required, hindering the design [5],[6]. Exact linearization strategy required that a large number of variables be measured [5]. Hysteresis control has the issue that a high value of the band leads to more distortion in current, while a low value increases the switching losses, furthermore it produces unpredictable harmonics, even when multi-band hysteresis strategy is used [5],[7],[8]. Popular modulation methods for CHB multilevel converters are sinusoidal pulse width modulation (SPWM) and Space Vector Modulation (SVM). SPWM, (when is used for multilevel converters, is also called multi-carrier based PWM), classified into two categories: phase-shifted modulation and level-shifted modulation, both require multiple triangular carriers [9]. SVM method is more complex when applied to more than three-level converters, due to the high number of space vectors and redundant switching states [10]. Finite control set model-based predictive control (FCS-MPC) is a well-established control technique for power converters due to its simplicity, fast dynamic response, ability to handle multivariable systems, nonlinearities and constraints [11]. When FCS-MPC strategy is implemented in multilevel CHB converters, it generates a variable switching frequency. Due to the finite number of possible switching states, the absence of a modulation stage in FCS-MPC becomes a disadvantage [12]. This generates noise as well as large voltage and current ripples deteriorating the performance of the system in terms of power quality [13],[14].

In this context, this paper examines the variable switching frequency causes by the implementation of FCS-MPC in a seven-level symmetric CHB DSTATCOM and proposes two different modulation stages to solve this issue. Also, to get better performance in terms of total harmonic distortion (THD), mean squared error (MSE), output voltages waveforms, and balance voltages on the capacitors.

This paper is organized as follows: Section II describes the three-phase seven-level CHB DSTATCOM topology. Section III expose FCS-MPC strategies with modulation stages proposed. Section IV illustrates the performance of the proposed techniques considering the simulation results. Finally, concluding remarks are presented in Section V.

II. SEVEN-LEVEL CHB DSTATCOM DESCRIPTION

Fig. 1 shows the DSTATCOM system under study. It is composed by $n_c = 3$ symmetric H-bridge cells per phase, that means that all voltages and capacitances of the capacitors have the same values, V_{dc} and C_{dc} , respectively. So, $l = 2n_c + 1 = 7$ levels of output voltage v_i^ϕ at the ac side can be obtained, where ϕ is the corresponding phase a , b or c . The addition of each cell output voltage v_i^ϕ , produces v_c^ϕ , where i is the corresponding cell 1, 2 or 3. Each v_i^ϕ depends on the states of the four switching devices that compose the cell. The states of the switching devices are represented by a binary signal s_{ij}^ϕ (0 for open and 1 for closed), where j is the corresponding switching device 1, 2, 3 or 4. Considering that switches 1 and 3 are always in opposite state with switches 2 and 4, respectively, only 2 signals (s_{i1}^ϕ and s_{i3}^ϕ) are needed to control one cell. Therefore, only the states listed below are allowed.

- $v_i^\phi = +V_{dc}$, when $s_{i1}^\phi = 1$ and $s_{i3}^\phi = 0$
- $v_i^\phi = 0$, when $s_{i1}^\phi = s_{i3}^\phi$
- $v_i^\phi = -V_{dc}$, when $s_{i1}^\phi = 0$ and $s_{i3}^\phi = 1$

Moreover, the seven-level CHB DSTATCOM of Fig. 1 has only $\varepsilon = 2^{2n_c} = 64$ possible switching states per phase. Each state (η^ϕ) can be represented by a numerical value F_s^ϕ , called switching function. Table I shows all possible switching states and their respective switching functions. The possible values of F_s^ϕ are 3, 2, 1, 0, -1, -2 and -3, which are the seven levels of the CHB DSTATCOM. It can be noted that there are switching states with the same value of the switching function, called redundant states, as shown in Table II. Then, the output voltage can be represented by the following equation:

$$v_c^\phi = F_s^\phi V_{dc} \quad (1)$$

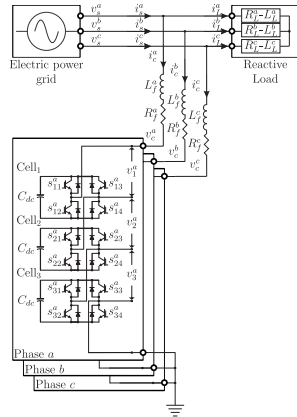


Fig. 1. Three-phase seven-level CHB DSTATCOM system.

TABLE I
SWITCHING FUNCTIONS FOR A SEVEN-LEVEL CHB DSTATCOM

s_{11}^ϕ	s_{13}^ϕ	s_{21}^ϕ	s_{23}^ϕ	s_{31}^ϕ	s_{33}^ϕ	η^ϕ	F_s^ϕ
0	0	0	0	0	0	1	0
0	0	0	0	0	1	2	-1
0	0	0	0	1	0	3	1
0	0	0	0	1	1	4	0
0	0	0	1	0	0	5	-1
0	0	0	1	0	1	6	-2
0	0	0	1	1	0	7	0
0	0	0	1	1	1	8	-1
0	0	1	0	0	0	9	1
0	0	1	0	0	1	10	0
0	0	1	0	1	0	11	2
0	0	1	0	1	1	12	1
0	0	1	1	0	0	13	0
0	0	1	1	0	1	14	-1
0	0	1	1	1	0	15	1
0	0	1	1	1	1	16	0
0	1	0	0	0	0	17	-1
0	1	0	0	0	1	18	-2
0	1	0	0	1	0	19	0
0	1	0	0	1	1	20	-1
0	1	0	1	0	0	21	-2
0	1	0	1	0	1	22	-3
0	1	0	1	1	0	23	-1
0	1	0	1	1	1	24	-2
0	1	1	0	0	0	25	0
0	1	1	0	0	1	26	-1
0	1	1	0	1	0	27	1
0	1	1	0	1	1	28	0
0	1	1	1	0	0	29	-1
0	1	1	1	0	1	30	-2
0	1	1	1	1	0	31	0
0	1	1	1	1	1	32	-1
1	0	0	0	0	0	33	1
1	0	0	0	0	1	34	0
1	0	0	0	1	0	35	2
1	0	0	0	1	1	36	1
1	0	0	1	0	0	37	0
1	0	0	1	0	1	38	-1
1	0	0	1	1	0	39	1
1	0	0	1	1	1	40	0
1	0	1	0	0	0	41	2
1	0	1	0	0	1	42	1
1	0	1	0	1	0	43	3
1	0	1	0	1	1	44	2
1	0	1	1	0	0	45	1
1	0	1	1	0	1	46	0
1	0	1	1	1	0	47	2
1	0	1	1	1	1	48	1
1	1	0	0	0	0	49	0
1	1	0	0	0	1	50	-1
1	1	0	0	1	0	51	1
1	1	0	0	1	1	52	0
1	1	0	1	0	0	53	-1
1	1	0	1	0	1	54	-2
1	1	0	1	1	0	55	0
1	1	0	1	1	1	56	-1
1	1	1	0	0	0	57	1
1	1	1	0	0	1	58	0
1	1	1	0	1	0	59	2
1	1	1	0	1	1	60	1
1	1	1	1	0	0	61	0
1	1	1	1	0	1	62	-1
1	1	1	1	1	0	63	1
1	1	1	1	1	1	64	0

TABLE II
AMOUNT OF REDUNDANT STATES FOR EACH LEVEL

Switching function	3	2	1	0	-1	-2	-3
Redundant states	1	6	15	20	15	6	1

III. PREDICTIVE CONTROL STRATEGY DESCRIPTION

Conventional FCS-MPC strategy for current control is formulated with a cost function that considers the output currents tracking error over one-step prediction horizon based on the system discrete model, called predictive model. Being the discrete model of the CHB DSTATCOM system:

$$i_{c[k+1]}^\phi = \left(1 - \frac{R_f T_s}{L_f}\right) i_{c[k]}^\phi + \frac{T_s}{L_f} (v_{s[k]}^\phi - v_{c[k]}^\phi) \quad (2)$$

where $i_{c[k+1]}^\phi$ are the predictions of the DSTATCOM phase currents made at sample k , T_s the sampling time, $i_{c[k]}^\phi$ are the currents injected by the DSTATCOM, $v_{s[k]}^\phi$ the grid voltages and k identifies the actual discrete-time sample.

The cost function is normally defined as the quadratic measure of the difference between the current reference and the predicted current as follows:

$$g_{[k+1]}^\phi = \|i_{c[k+1]}^{\phi*} - i_{c[k+1]}^\phi\|^2 \quad (3)$$

where the superscript (*) denotes the reference variables.

The switching function (that is, the switching state) that gets a minimum cost function value is selected by an optimization process. Once the optimization process time is finished, the optimal switching state (η_{opt}^ϕ , where the subscript opt denotes optimal) is applied to the CHB DSTATCOM for the rest of the sampling period until the calculation time of the next optimal switching state ends. Ideally, the calculation time is negligible.

A. Delay compensation

The optimization process is carried out through an exhaustive search in all possible switching states. During the optimization process, predictive currents [Eq. (2)] and cost function [Eq. (3)] must be computed $\varepsilon = 64$ times at each T_s to guarantee optimality. This way, the computation time can be significant compared with T_s (this obviously depends on the sampling frequency and the computation speed of the controller). As a consequence, the measured currents and voltages at the beginning of the sampling time, which are used in the optimization process, are not valid for the end of sampling time due to the computation time delay. Then it is necessary to carry out a second prediction step as follows:

$$i_{c[k+2]}^\phi = \left(1 - \frac{R_f T_s}{L_f}\right) i_{c[k+1]}^\phi + \frac{T_s}{L_f} (v_{s[k+1]}^\phi - v_{c[k+1]}^\phi) \quad (4)$$

and

$$g_{[k+2]}^\phi = \|i_{c[k+2]}^{\phi*} - i_{c[k+2]}^\phi\|^2 \quad (5)$$

where $i_{c[k+1]}^\phi$ is calculated from Eq. (2) using measured DSTATCOM currents $i_{c[k]}^\phi$ and considering the CHB DSTATCOM phase voltages $v_{c[k]}^\phi$ selected by the predictive control in the previous sampling period.

B. Modulation stage

1) Phase shift carrier pulse width modulation (PSC-PWM):

In general, CHB DSTATCOMs with n_c cells, requires n_c phase shifted triangular carrier waves per phase. For this modulation, all carriers have the same frequency and magnitude peak to peak, but the phase shift between two adjacent carriers is given by $\theta = 180^\circ/n_c$. The activation signals s_{11}^ϕ and s_{33}^ϕ are generated by comparing one specific carrier wave $v_{cr,i}^\phi$ with a pair of inverted modulation signals v_{cont}^ϕ and $-v_{cont}^\phi$ respectively. Fig. 2 describe how the activation signals are obtained, considering the carrier frequency (f_{cr}) equal to the sampling frequency (f_s). The modulating signals are associated with the CHB DSTATCOM phase voltages and are normalized between -1 and 1 as follows:

$$v_{cont}^\phi = \frac{v_{c,opt}^\phi}{3V_{dc}} \quad (6)$$

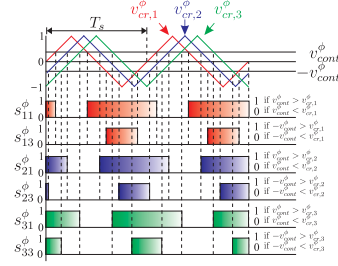


Fig. 2. PSC-PWM scheme for CHB DSTATCOM phase ϕ .

a) *Optimization process:* The optimization process for FCS-MPC with PSC-PWM is summarizing in Algorithm 1. FCS-MPC technique selects the $v_{cont,opt}^\phi$ of 7 possible levels. So, Eq. (4) and Eq. (5) must be computed only 7 times at each T_s . PSC-PWM technique is only responsible for determining the switching states and their respective duty cycles, as shown in Fig. 2.

Algorithm 1 Optimization algorithm of FCS-MPC with PSC-PWM

1. Initialize $g_{opt}^\phi := \infty, n := 0$
2. Compute the DSTATCOM reference currents $i_{c[k+2]}^{\phi*}$
3. Compute the first prediction [Eq. (2)]
4. **while** $n \leq l$ **do**
5. Compute the second prediction [Eq. (4)]
6. Compute the cost function [Eq. (5)]
7. **if** $g^\phi < g_{opt}^\phi$ **then**
8. $g_{opt}^\phi \leftarrow g^\phi, v_{c,opt}^\phi \leftarrow v_c^\phi$
9. **end if**
10. $n := n + 1$
11. **end while**
12. Compute the modulation signal [Eq. (6)]

2) *Space state modulation (SSM)*: The SSM technique has a procedure similar to the SVM. In SVM, each sector is defined by two adjacent active (not null) vectors. In the proposed SSM, the “sectors” are composed of two consecutive active switching states (states with $F_s^\phi \neq 0$). “sector 1” is composed of states $\eta = 2$ and $\eta = 3$, “sector 2” is composed of states $\eta = 3$ and $\eta = 5$, and so on (refer to Table I). The optimum sector ($\eta_{1,opt}^\phi$ and $\eta_{2,opt}^\phi$) is selected by an optimization process that calculates the cost functions (g_1^ϕ and g_2^ϕ) defined by Eq. (3) separately for each prediction ($i_{c1[k+1]}^\phi$ and $i_{c2[k+1]}^\phi$). If the value of g_1^ϕ is lower than g_2^ϕ , the switching state $\eta_{1,opt}^\phi$ must be applied for a longer time than the switching state $\eta_{2,opt}^\phi$, and vice versa. This is simply because a lower value of the cost function means less tracking error, as a result, the reference is reached in less time. Therefore, duty cycles (τ_1^ϕ and τ_2^ϕ) must be inversely proportional to their respective cost functions, as follows:

$$\begin{aligned} \tau_0^\phi &= K/g_0^\phi \\ \tau_1^\phi &= K/g_1^\phi \\ \tau_2^\phi &= K/g_2^\phi \\ \tau_0^\phi + \tau_1^\phi + \tau_2^\phi &= 1 \end{aligned} \quad (7)$$

where τ_0^ϕ is the duty cycle of a switching state (η_0^ϕ) with $F_s^\phi = 0$ ($\eta = 1$, arbitrarily chosen) and K is a constant of proportionality and the expressions of the duty cycles for each switching state are given solving Eq. (7) for K as:

$$\begin{aligned} \tau_0^\phi &= g_1^\phi g_2^\phi / (g_0^\phi g_1^\phi + g_1^\phi g_2^\phi + g_0^\phi g_2^\phi) \\ \tau_1^\phi &= g_0^\phi g_2^\phi / (g_0^\phi g_1^\phi + g_1^\phi g_2^\phi + g_0^\phi g_2^\phi) \\ \tau_2^\phi &= g_0^\phi g_1^\phi / (g_0^\phi g_1^\phi + g_1^\phi g_2^\phi + g_0^\phi g_2^\phi) \end{aligned} \quad (8)$$

a) *New cost function*: The new cost function is defined as the weighted sum of the cost functions g_1^ϕ and g_2^ϕ , where the weighting factors are τ_1^ϕ and τ_2^ϕ given by Eq. (8), as:

$$g_{[k+1]}^\phi = \tau_1^\phi g_{1[k+1]}^\phi + \tau_2^\phi g_{2[k+1]}^\phi \quad (9)$$

b) *New optimization process*: Since there are $\varrho = 44$ sectors (44 active switching state), Eq. (2), Eq. (3) and Eq. (8), for η_1^ϕ and η_2^ϕ , and Eq. (9), must be computed 44 times at each T_s . The optimization process for FCS-MPC with SSM is illustrated in Algorithm 2. It should be noted that g_0^ϕ is computed only once. It is assumed that the computational cost of FCS-MPC with SSM is higher than FCS-MPC with PSC-PWM, due to the fact that FCS-MPC with SSM needs more calculation process to obtain the optimal sector.

c) *Switching pattern*: The switching states $\eta_{1,opt}^\phi$, $\eta_{2,opt}^\phi$ and $\eta_{0,opt}^\phi$ are applied using the switching pattern procedure that is shown in Fig.3, where their respective turn-on times are given by:

$$\begin{aligned} T_0^\phi &= \tau_0^\phi T_s \\ T_1^\phi &= \tau_1^\phi T_s \\ T_2^\phi &= \tau_2^\phi T_s \end{aligned} \quad (10)$$

Algorithm 2 Optimization algorithm of FCS-MPC with SSM

1. Initialize $g_{opt}^\phi := \infty, n := 0$
2. Compute the DSTATCOM reference currents $i_{c[k+1]}^{\phi*}$
3. Compute the first prediction and the cost function for η_0^ϕ
4. **while** $n \leq \varrho$ **do**
5. Compute the first prediction for η_1^ϕ and η_2^ϕ
6. Compute the cost function for η_1^ϕ and η_2^ϕ
7. Compute the duty cycles [Eq. (8)]
8. Compute the new cost function [Eq. (9)]
9. **if** $g^\phi < g_{opt}^\phi$ **then**
10. $g_{opt}^\phi \leftarrow g^\phi, \eta_{1,opt}^\phi \leftarrow \eta_1^\phi, \eta_{2,opt}^\phi \leftarrow \eta_2^\phi$
11. **end if**
12. $n := n + 1$
13. **end while**

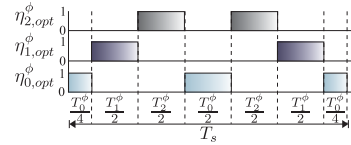


Fig. 3. Switching pattern for the optimal switching states.

IV. SIMULATION RESULTS AND DISCUSSION

Simulation results are presented to compare the performance of the proposed methods, considering the sampling and carriers frequencies of 10 kHz ($f_{cr} = f_s$). For a more fair comparison, 5 kHz is used for FCS-MPC with SSM. Matlab/Simulink environment was used for simulations, considering the electrical parameters shown in Table III. A numerical integration based on Ode4 Runge-Kutta was used for the computation of fixed-step in the time domain.

TABLE III
PARAMETERS DESCRIPTION

PARAMETER	Electric power grid		
	SYMBOL	VALUE	UNIT
Grid frequency	f_e	50	Hz
Grid voltage	v_s	310.2	V
seven-Level CHB DSTATCOM			
Filter resistance	R_f	0.09	Ω
Filter inductance	L_f	3	mH
dc-link voltage	V_{dc}	114	V
dc-link capacitance	C_{dc}	680	μF
Load parameters			
Load resistance	R_L	23.2	Ω
Load inductance	L_L	55	mH
Predictive control parameters			
Sampling time	T_s	100	μs
Simulation step	—	1	μs
Ideal active power reference	P_c^*	0	W
Ideal reactive power reference	Q_c^*	$Q_L = 3\,000$	VAR

The MSE between the reference and the measured value of the current injected by the DSTATCOM [Eq. (11)], and the THD of the CHB DSTATCOM output voltage and the grid current [Eq. (12)] have been used as quality performance indices to compare quantitatively the proposed methods.

$$\text{MSE}(\Psi) = \sqrt{\frac{1}{N} \sum_{j=1}^N \Psi_j^2} \quad (11)$$

$$\text{THD} = \sqrt{\frac{1}{x_1^2} \sum_{i=2}^N x_i^2} \quad (12)$$

being Ψ the tracking current error, N the number of elements, x_1 the amplitude of the fundamental frequency of the analyzed variable, and x_i the variable harmonics. Being the range of interest from 0.03 s to 0.07 s (two cycles) and, considering the simulation step of 1 μ s, result in 40000 samples for the calculation of the MSE and THD parameters.

The current references are calculated taking in account the ideal active a reactive power references [Table III], to obtain a unit power factor at the grid side, and assuming that the DSTATCOM does not consume active power. The MSE parameter of current tracking i_a^* for the proposed methods, can be seen in Fig. 4 (a) to (c). MSE parameter obtained with the conventional FCS-MPC technique gives a value of 0.9628 A [Fig. 4 (a)]. The FCS-MPC with PSC-PWM method reduce the MSE parameter from 0.9628 A to 0.8901 A (about 7.55 %) [Fig. 4 (b)]. The FCS-MPC with SSM method reduce the MSE parameter from 0.9628 A to 0.5987 A (about 38 %) [Fig. 4 (c)].

The THD parameter of the CHB DSTATCOM output voltage v_c^* and the THD parameter of the grid current i_a^* , for the proposed methods, can be seen in Fig. 5 (a) to (c) and Fig. 6 (a) to (c), respectively. The THD parameter of v_c^* obtained with the conventional FCS-MPC technique gives a value of 29.41 % [Fig. 5 (a)]. The FCS-MPC with PSC-PWM method slightly increase the THD parameter from 29.41 % to 29.65 % [Fig. 5 (b)]. The FCS-MPC with SSM method reduce the THD parameter from 29.41 % to 25.22 % [Fig. 5 (c)]. It can also be seen that the operation at fixed switching frequency (FCS-MPC with SSM method) produce a dominant harmonic (of 5 kHz and its multiples) which is the fixed switching frequency of the CHB DSTATCOM. Regarding the grid current i_a^* , the THD parameter obtained with the conventional FCS-MPC technique gives a value of 13.38 % [Fig. 6 (a)]. The FCS-MPC with PSC-PWM method reduce the THD parameter from 13.38 % to 12.47 % [Fig. 6 (b)]. The FCS-MPC with SSM method reduce the THD parameter from 13.38 % to 9.19 % [Fig. 6 (c)]. A more concentrated spectrum is obtained with the FCS-MPC with SSM technique.

With respect to the voltage evolution on the capacitors in phase a , all voltage remain constant until instant 0.02 s, when the CHB DSTATCOM is connected. A better performance is obtained in terms of voltage ripple and a simultaneous charge/discharge process on the capacitors using the

FCS-MPC with PSC-PWM technique, as shown in Fig. 6 (b) compared with the conventional FCS-MPC [Fig. 6 (a)] and the FCS-MPC with SSM [Fig. 6 (c)] techniques. Similar results for phases b and c , are summarized in Table IV.

V. CONCLUSION

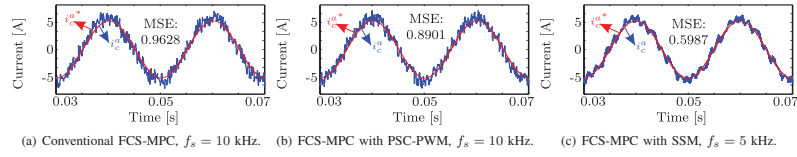
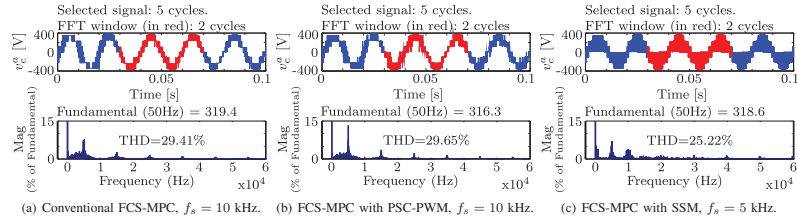
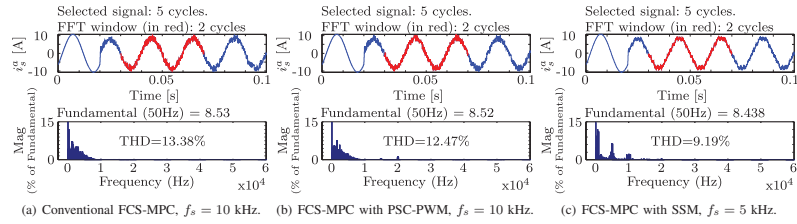
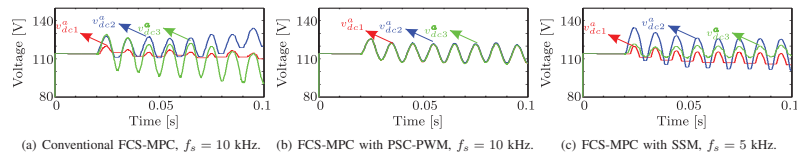
Simulation results show that it is possible to increase the performance of the conventional FCS-MPC in terms of MSE and THD parameters, thanks to the inclusion of different modulation stages. A better performance is obtained with FCS-MPC with SSM. However, FCS-MPC with PSC-PWM have a lower computational cost and, relative to balance voltages on the capacitors, presents a better performance.

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Fig. 4. Mean square error for current tracking in phase a .Fig. 5. THD of the CHB DSTATCOM output voltage in phase a .Fig. 6. THD of the grid current in phase a .Fig. 7. Voltage evolution on the capacitors in phase a .TABLE IV
SIMULATION RESULTS FOR PHASES b AND c

PARAMETER	Conventional FCS-MPC ($f_s = 10$ kHz)		FCS-MPC with PSC-PWM ($f_s = 10$ kHz)		FCS-MPC with SSM ($f_s = 5$ kHz)	
	PHASE b	PHASE c	PHASE b	PHASE c	PHASE b	PHASE c
MSE for current tracking	0.9700	0.8899	0.8752	0.8997	0.6354	0.5617
THD of the output voltage	29.82%	31.03%	33.22%	44.00%	25.34%	24.96%
THD of the grid current	12.91%	12.41%	11.88%	13.09%	8.75%	8.52%

